

# **UHF FM/AM Transmitter**

The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems. They include a Colpitts crystal reference oscillator, UHF oscillator, + 8 (MC13175) or + 32 (MC13176) prescaler and phase detector forming a versatile PLL system. Targeted applications are in the 260 to 470 MHz band and 902 to 928 MHz band covered by FCC Title 47; Part 15. Other applications include local oscillator sources in UHF and 900 MHz receivers, UHF and 900 MHz video transmitters, RF Local Area Networks (LANs), and high frequency clock drivers. The MC13175/76 offer the following features:

- UHF Current Controlled Oscillator
- Uses Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Fewer External Parts Required
- Low Operating Supply Voltage (1.8 to 5.0 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output On and Off
- (MC13175) f<sub>0</sub> = 8 x f<sub>ref</sub>; (MC13176) f<sub>0</sub> = 32 x f<sub>ref</sub>



# UHF FM/AM TRANSMITTER

SEMICONDUCTOR TECHNICAL DATA



PLASTIC PACKAGE CASE 751B (SO–16)





### **ORDERING INFORMATION**

Device	Operating Temperature Range	Package
MC13175D		SO-16
MC13176D	$I_{A} = -40$ to +05 C	SO-16

## **MAXIMUM RATINGS** ( $T_A = 25^{\circ}C$ , unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	VCC	7.0 (max)	Vdc
Operating Supply Voltage Range	VCC	1.8 to 5.0	Vdc
Junction Temperature	ТJ	+150	°C
Operating Ambient Temperature	TA	- 40 to + 85	°C
Storage Temperature	T <sub>stg</sub>	- 65 to +150	°C

## **ELECTRICAL CHARACTERISTICS** (Figure 2; $V_{EE} = -3.0$ Vdc, $T_A = 25^{\circ}C$ , unless otherwise noted.)\*

Characteristic	Pin	Symbol	Min	Тур	Max	Unit
Supply Current (Power down: I <sub>11</sub> & I <sub>16</sub> = 0)	-	I <sub>EE1</sub>	- 0.5	-	_	μΑ
Supply Current (Enable [Pin 11] to V <sub>CC</sub> thru 30 k, I <sub>16</sub> = 0)	-	I <sub>EE2</sub>	-18	-14	_	mA
Total Supply Current (Transmit Mode) (I <sub>mod</sub> = 2.0 mA; f <sub>o</sub> = 320 MHz)	_	IEE3	- 39	- 34	_	mA
$ \begin{array}{l} \mbox{Differential Output Power} (f_0 = 320 \mbox{ MHz; } V_{ref} \mbox{[Pin 9]} \\ = 500 \mbox{ mV}_{p-p}; f_0 = N \mbox{ x } f_{ref}) \\ \mbox{I}_{mod} = 2.0 \mbox{ mA} \mbox{ (see Figure 7, 8)} \\ \mbox{I}_{mod} = 0 \mbox{ mA} \end{array} $	13 & 14	Pout	2.0 _	+ 4.7 - 45	-	dBm
Hold–in Range (± ∆f <sub>ref</sub> x N) MC13175 (see Figure 7) MC13176 (see Figure 8)	13 & 14	$\pm \Delta f H$	3.5 4.0	6.5 8.0	-	MHz
Phase Detector Output Error Current MC13175 MC13176	7	lerror	20 22	25 27		μΑ
Oscillator Enable Time (see Figure 22b)	11 & 8	<sup>t</sup> enable	-	4.0	—	ms
Amplitude Modulation Bandwidth (see Figure 24)	16	BWAM	-	25	—	MHz
Spurious Outputs (I <sub>mod</sub> = 2.0 mA) Spurious Outputs (I <sub>mod</sub> = 0 mA)	13 & 14 13 & 14	P <sub>son</sub> P <sub>soff</sub>	-	- 50 - 50	_	dBc
Maximum Divider Input Frequency Maximum Output Frequency	_ 13 & 14	f <sub>div</sub> f <sub>o</sub>	-	950 950	_	MHz

 $^{\ast}$  For testing purposes, V<sub>CC</sub> is ground (see Figure 2).





3. Recommended source is Coilcraft "slot seven" inductor, part number 7M3-821.

## **PIN FUNCTION DESCRIPTIONS**

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1 & 4	Osc 1, Osc 4	10k 10k 10k 0sc 4	<b>CCO Inputs</b> The oscillator is a current controlled type. An external oscillator coil is connected to Pins 1 and 4 which forms a parallel resonance LC tank circuit with the internal capacitance of the IC and with parasitic capacitance of the PC board. Three base–emitter capacitances in series configuration form the capacitance for the parallel tank. These are the base–emitters at Pins 1 and 4 and the base–emitter of the differential amplifier. The equivalent series capacitance in the differential amplifier is varied by the modulating current from the frequency control circuit (see Pin 6, internal circuit). A more thorough discussion is found in the Applications Information section.
5	VEE	VEE 5 Subcon VEE = VEE =	Supply Ground (VEE) In the PCB layout, the ground pins (also applies to Pins 10 and 15) should be connected directly to chassis ground. Decoupling capacitors to $V_{CC}$ should be placed directly at the ground returns.
6	ICont	6 ICont E	<b>Frequency Control</b> For V <sub>CC</sub> = 3.0 Vdc, the voltage at Pin 6 is approximately 1.55 Vdc. The oscillator is current controlled by the error current from the phase detector. This current is amplified to drive the current source in the oscillator section which controls the frequency of the oscillator. Figures 9 and 10 show the $\Delta f_{OSC}$ versus I <sub>Cont</sub> , Figure 5 shows the $\Delta f_{OSC}$ versus I <sub>Cont</sub> at – 40°C, + 25°C and + 85°C for 320 MHz. The CCO may be FM modulated as shown in Figure 17, MC13176 320 MHz FM Transmitter. A detailed discussion is found in the Applications Information section.
7	PD <sub>out</sub>	V <sub>CC</sub> 4.0k 4.0k PD <sub>out</sub> 7	<b>Phase Detector Output</b> The phase detector provides $\pm$ 30 µA to keep the CCO locked at the desired carrier frequency. The output impedance of the phase detector is approximately 53 k $\Omega$ . Under closed loop conditions there is a DC voltage which is dependent upon the free running oscillator and the reference oscillator frequencies. The circuitry between Pins 7 and 6 should be selected for adequate loop filtering necessary to stabilize and filter the loop response. Low pass filtering between Pin 7 and 6 is needed so that the corner frequency is well below the sum of the divider and the reference oscillator frequencies, but high enough to allow for fast response to keep the loop locked. Refer to the Applications Information section regarding loop filtering and FM modulation.

## **PIN FUNCTION DESCRIPTIONS**

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
9	Xtale Xtalb	V <sub>CC</sub> 9 Xtalb 8 C Xtale -	<b>Crystal Oscillator Inputs</b> The internal reference oscillator is configured as a common emitter Colpitts. It may be operated with either a fundamental or overtone crystal depending on the carrier frequency and the internal prescaler. Crystal oscillator circuits and specifications of crystals are discussed in detail in the applications section. With $V_{CC} = 3.0$ Vdc, the voltage at Pin 8 is approximately 1.8 Vdc and at Pin 9 is approximately 2.3 Vdc. 500 to 1000 mVp–p should be present at Pin 9. The Colpitts is biased at 200 $\mu$ A; additional drive may be acquired by increasing the bias to approximately 500 $\mu$ A. Use 6.2 k from Pin 8 to ground.
10	Reg. Gnd	V <sub>CC</sub> 5.0p Reg	<b>Regulator Ground</b> An additional ground pin is provided to enhance the stability of the system. Decoupling to the $V_{CC}$ (RF ground) is essential; it should be done at the ground return for Pin 10.
11	Enable	11 O Enable Subcon = 10 O Reg. Gnd	<b>Device Enable</b> The potential at Pin 11 is approximately 1.25 Vdc. When Pin 11 is open, the transmitter is disabled in a power down mode and draws less than 1.0 $\mu$ A I <sub>CC</sub> if the MOD at Pin 16 is also open (i.e., it has no current driving it). To enable the transmitter a current source of 10 $\mu$ A to 90 $\mu$ A is provided. Figures 3 and 4 show the relationship between I <sub>CC</sub> , V <sub>CC</sub> and I <sub>reg.</sub> enable. Note that I <sub>CC</sub> is flat at approximately 10 mA for I <sub>reg.</sub> enable = 5.0 to 100 $\mu$ A (I <sub>mod</sub> = 0).
12	VCC	V <sub>CC</sub> 12 V <sub>CC</sub>	Supply Voltage (V <sub>CC</sub> ) The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V <sub>CC</sub> trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
13 & 14	Out 1 and Out 2	V <sub>CC</sub>	<b>Differential Output</b> The output is configured differentially to easily drive a loop antenna. By using a transformer or balun, as shown in the application schematic, the device may then drive an unbalanced low impedance load. Figure 6 shows how much the Output Power and Free–Running Oscillator Frequency change with temperature at 3.0 Vdc; I <sub>mod</sub> = 2.0 mA.
15	Out_Gnd	13 0ut 1 0ut 2 14 16 1mod	<b>Output Ground</b> This additional ground pin provides direct access for the output ground to the circuit board $V_{\mbox{EE}}$ .
16	Imod	The second secon	AM Modulation/Power Output Level The DC voltage at this pin is 0.8 Vdc with the current source active. An external resistor is chosen to provide a source current of 1.0 to 3.0 mA, depending on the desired output power level at a given $V_{CC}$ . Figure 23 shows the relationship of Power Output to Modulation Current, $I_{Mod}$ . At $V_{CC}$ = 3.0 Vdc, 3.5 dBm power output can be acquired with about 35 mA I <sub>CC</sub> . For FM modulation, Pin 16 is used to set the desired output power level as described above. For AM modulation, the modulation signal must ride on a positive DC bias offset which sets a static (modulation off) modulation current. External circuitry for various schemes is further discussed in the Applications Information section.





**APPLICATIONS INFORMATION** 

## Evaluation PC Board

The evaluation PCB, shown in Figures 26 and 27, is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 28 and 29). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

## Current Controlled Oscillator (Pins 1 to 4)

It is critical to keep the interconnect leads from the CCO (Pins 1 and 4) to the external inductor symmetrical and equal in length. With a minimum inductor, the maximum free running frequency is greater than 1.0 GHz. Since this inductor will be small, it may be either a microstrip inductor, an air wound inductor or a tuneable RF coil. An air wound inductor may be tuned by spreading the windings, whereas tuneable RF coils are tuned by adjusting the position of an aluminum core in a threaded coilform. As the aluminum core coupling to the windings is increased, the inductance is decreased. The temperature coefficient using an aluminum cores made by Coilcraft may be obtained with aluminum cores (Part No. 51–129–169).

## Ground (Pins 5, 10 and 15)

**Ground Returns:** It is best to take the grounds to a backside ground plane via plated through holes or eyelets at the pins. The application PCB layout implements this technique. Note that the grounds are located at or less than 100 mils from the devices pins.

**Decoupling:** Decoupling each ground pin to  $V_{CC}$  isolates each section of the device by reducing interaction between sections and by localizing circulating currents.

## Loop Characteristics (Pins 6 and 7)

Figure 11 is the component block diagram of the MC1317XD PLL system where the loop characteristics are described by the gain constants. Access to individual components of this PLL system is limited, inasmuch as the loop is only pinned out at the phase detector output and the

frequency control input for the CCO. However, this allows for characterization of the gain constants of these loop components. The gain constants  $K_p$ ,  $K_o$  and  $K_n$  are well defined in the MC13175 and MC13176.

## Phase Detector (Pin 7)

With the loop in lock, the difference frequency output of the phase detector is DC voltage that is a function of the phase difference. The sinusoidal type detector used in this IC has the following transfer characteristic:

## $I_e = A \sin \theta_e$

The gain factor of the phase detector, K<sub>p</sub> (with the loop in lock) is specified as the ratio of DC output current,  $l_e$  to phase error,  $\theta_e$ :

$$\begin{split} & \mathsf{K}_p = \mathsf{I}_e/\theta_e \; (\mathsf{Amps/radians}) \\ & \mathsf{K}_p = \mathsf{A} \; \mathsf{Sin} \; \theta_e/\theta_e \\ & \mathsf{Sin} \; \theta_e \sim \theta_e \; \mathsf{for} \; \theta_e \leq 0.2 \; \mathsf{radians}; \\ & \mathsf{thus}, \; \mathsf{K}_p = \mathsf{A} \; (\mathsf{Amps/radians}) \end{split}$$

Figures 7 and 8 show that the detector DC current is approximately 30  $\mu$ A where the loop loses lock at  $\theta_e = \pm \pi/2$  radians; therefore, K<sub>p</sub> is 30  $\mu$ A/radians.

## Current Controlled Oscillator, CCO (Pin 6)

Figures 9 and 10 show the non-linear change in frequency of the oscillator over an extended range of control current for 320 and 450 MHz applications. Ko ranges from approximately 6.3x10<sup>5</sup> rad/sec/µA or 100 kHz/µA (Figure 9) to 8.8x10<sup>5</sup> rad/sec/µA or 140 kHz/µA (Figure 10) over a relatively linear response of control current (0 to 100 µA). The oscillator gain factor depends on the operating range of the control current (i.e., the slope is not constant). Included in the CCO gain factor is the internal amplifier which can sink and source at least 30 µA of input current from the phase detector. The internal circuitry at Pin 6 limits the CCO control current to 50 µA of source capability while its sink capability exceeds 200 µA as shown in Figures 9 and 10. Further information to follow shows how to use the full capabilities of the CCO by addition of an external loop amplifier and filter (see Figure 15). This additional circuitry yields at  $K_0 =$ 0.145 MHz/μA or 9.1x10<sup>5</sup> rad/sec/μA.

### Figure 11. Block Diagram of MC1317XD PLL



#### Loop Filtering

The fundamental loop characteristics, such as capture range, loop bandwidth, lock–up time and transient response are controlled externally by loop filtering.

The natural frequency  $(\omega_n)$  and damping factor ( $\partial$ ) are important in the transient response to a step input of phase or frequency. For a given  $\partial$  and lock time,  $\omega_n$  can be determined from the plot shown in Figure 12.



Figure 12. Type 2 Second Order Response

 $\begin{array}{lll} \mbox{Where:} & \mbox{K}_p = \mbox{Phase detector gain constant in} & \mbox{$\mu$A/rad$}; \mbox{$K_p$} = 30 \mbox{$\mu$A/rad$} & \mbox{$K_f$} = \mbox{Filter transfer function} & \mbox{$K_n$} = \mbox{$1/N$}; \mbox{$N = 8$ for the MC13175 and} & \mbox{$K_0$} & \mbox{$N = 32$ for the MC13176} & \mbox{$= CCO$ gain constant in rad/sec/$\mu$A} & \mbox{$K_0 = $9.1 \times 10^5$ rad/sec/$\mu$A} \end{array}$ 

For  $\partial = 0.707$  and lock time = 1.0 ms; then  $\omega_n = 5.0/t = 5.0$  krad/sec.

The loop filter may take the form of a simple low pass filter or a lag-lead filter which creates an additional pole at origin in the loop transfer function. This additional pole along with that of the CCO provides two pure integrators (1/s<sup>2</sup>). In the lag-lead low pass network shown in Figure 13, the values of the low pass filtering parameters R<sub>1</sub>, R<sub>2</sub> and C determine the loop constants  $\omega_n$  and  $\partial$ . The equations  $t_1 = R_1C$  and  $t_2 = R_2C$  are related in the loop filter transfer functions F(s) = 1 + t\_2s/1 + (t\_1 + t\_2)s.

#### Figure 13. Lag–Lead Low Pass Filter



The closed loop transfer function takes the form of a 2nd order low pass filter given by,

$$H(s) = K_V F(s)/s + K_V F(s)$$

From control theory, if the loop filter characteristic has F(0) = 1, the DC gain of the closed loop,  $K_V$  is defined as,

$$K_v = K_p K_0 K_n$$

and the transfer function has a natural frequency,

$$\omega_{\rm n} = (K_{\rm v}/t_1 + t_2)^{1/2}$$

and a damping factor,

 $\partial = (\omega_{\rm D}/2) (t_2 + 1/K_{\rm V})$ 

Rewriting the above equations and solving for the MC13176 with  $\partial$  = 0.707 and  $\omega_{D}$  = 5.0 k rad/sec:

$$\begin{array}{l} {\sf K}_V = {\sf K}_{P} {\sf K}_0 {\sf K}_{\Pi} = (30) \; (0.91 \, \times \, 10^6) \; (1/32) = 0.853 \, \times \, 10^6 \\ t_1 + t_2 = {\sf K}_V / \omega_{\Pi} 2 = 0.853 \, \times \, 10^6 / (25 \, \times \, 106) = 34.1 \; \text{ms} \\ t_2 = 2\partial / \omega_{\Pi} = (2) \; (0.707) / (5 \, \times \, 10^3) = 0.283 \; \text{ms} \\ t_1 = ({\sf K}_V / \omega_{\Pi} 2) - t_2 = (34.1 - 0.283) = 33.8 \; \text{ms} \end{array}$$

For  $C = 0.47 \mu$ ;

then, R<sub>1</sub> = t<sub>1</sub>/C =  $33.8 \times 10^{-3}/0.47 \times 10^{-6}$  = 72 k dthus, R<sub>2</sub> = t<sub>2</sub>/C =  $0.283 \times 10^{-3}/0.47 \times 10^{-6}$  = 0.60 k In the above example, the following standard value components are used,

C = 0.47  $\mu$ ; R<sub>2</sub> = 620 and R'<sub>1</sub> = 72 k - 53 k ~ 18 k

 $(R'_1 \text{ is defined as } R_1 - 53 \text{ k}$ , the output impedance of the phase detector.)

Since the output of the phase detector is high impedance (~50 k) and serves as a current source, and the input to the frequency control, Pin 6 is low impedance (impedance of the two diode to ground is approximately 500  $\Omega$ ), it is imperative that the second order low pass filter design above be modified. In order to minimize loading of the R<sub>2</sub>C shunt network, a higher impedance must be established to Pin 6. A simple solution is achieved by adding a low pass network between the passive second order network and the input to Pin 6. This helps to minimize the loading effects on the second order low pass while further suppressing the sideband spurs of the crystal oscillator. A low pass filter with R<sub>3</sub> = 1.0 k and C<sub>2</sub> = 1500 p has a corner frequency (f<sub>c</sub>) of 106 kHz; the reference sideband spurs are down greater than – 60 dBc.

### Figure 14. Modified Low Pass Loop Filter



### Hold-In Range

The hold–in range, also called the lock range, tracking range and synchronization range, is the ability of the CCO frequency,  $f_0$  to track the input reference signal,  $f_{ref} \bullet N$  as it gradually shifted away from the free running frequency,  $f_f$ . Assuming that the CCO is capable of sufficient frequency deviation and that the internal loop amplifier and filter are not overdriven, the CCO will track until the phase error,  $\theta_e$  approaches  $\pm \pi/2$  radians. Figures 5 through 8 are a direct

measurement of the hold–in range (i.e.  $\Delta f_{ref} \times N = \pm \Delta f_H \times 2\pi$ ). Since sin  $\theta_e$  cannot exceed ±1.0, as  $\theta_e$  approaches  $\pm \pi/2$  the hold–in range is equal to the DC loop gain, K<sub>V</sub> × N.

$$\pm \Delta \omega_{\rm H} = \pm K_{\rm V} \times N$$

where, 
$$K_V = K_p K_0 K_{n.}$$

In the above example,

 $\pm \Delta \omega_{\text{H}} = \pm 27.3 \text{ Mrad/sec}$  $\pm \Delta f_{\text{H}} = \pm 4.35 \text{ MHz}$ 

### **Extended Hold-in Range**

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The hold-in range of about 3.4% could cause problems over temperature in cases where the free-running oscillator drifts more than 2 to 3% because of relatively high temperature coefficients of the ferrite tuned CCO inductor. This problem might worsen for lower frequency applications where the external tuning coil is large compared to internal capacitance at Pins 1 and 4. To improve hold-in range performance, it is apparent that the gain factors involved must be carefully considered.

- $K_n$  = is either 1/8 in the MC13175 or 1/32 in the MC13176.
- $K_p$  = is fixed internally and cannot be altered.
- $K_0$  = Figures 9 and 10 suggest that there is capability of greater control range with more current swing. However, this swing must be symmetrical about the center of the dynamic response. The suggested zero current operating point for ±100 µA swing of the CCO is at about + 70 µA offset point.
- Ka = External loop amplification will be necessary since the phase detector only supplies  $\pm$  30  $\mu$ A.

In the design example in Figure 15, an external resistor (R<sub>5</sub>) of 15 k to V<sub>CC</sub> (3.0 Vdc) provides approximately 100  $\mu$ A of current boost to supplement the existing 50  $\mu$ A internal source current. R<sub>4</sub> (1.0 k) is selected for approximately 0.1 Vdc across it with 100  $\mu$ A. R<sub>1</sub>, R<sub>2</sub> and R<sub>3</sub> are selected to set the potential at Pin 7 and the base of 2N4402 at approximately 0.9 Vdc and the emitter at 1.55 Vdc when error current to Pin 6 is approximately zero  $\mu$ A. C<sub>1</sub> is chosen to reduce the level of the crystal sidebands.

### Figure 15. External Loop Amplifier



Figure 16 shows the improved hold–in range of the loop. The  $\Delta f_{ref}$  is moved 950 kHz with over 200  $\mu A$  swing of control current for an improved hold–in range of ±15.2 MHz or ± 95.46 Mrad/sec.



### Lock-in Range/Capture Range

If a signal is applied to the loop not equal to free running frequency,  $f_f$ , then the loop will capture or lock-in the signal by making  $f_S$  =  $f_O$  (i.e. if the initial frequency difference is not too great). The lock-in range can be expressed as  $\Delta\omega_L$  ~  $\pm$   $2\partial\omega_R$ 

### **FM Modulation**

Noise external to the loop (phase detector input) is minimized by narrowing the bandwidth. This noise is minimal in a PLL system since the reference frequency is usually derived from a crystal oscillator. FM can be achieved by applying a modulation current superimposed on the control current of the CCO. The loop bandwidth must be narrow enough to prevent the loop from responding to the modulation frequency components, thus, allowing the CCO to deviate in frequency. The loop bandwidth is related to the natural frequency  $\omega_n$ . In the lag–lead design example where the natural frequency,  $\omega_n = 5.0$  krad/sec and a damping factor,  $\partial = 0.707$ , the loop bandwidth = 1.64 kHz. Characterization data of the closed loop responses for both the MC13175 and MC13176 at 320 MHz (Figures 7 and 8, respectively) show satisfactory performance using only a simple low-pass loop filter network. The loop filter response is strongly influenced by the high output impedance of the push-pull current output of the phase detector.

 $f_{c} = 0.159/RC;$ 

For R = 1.0 k + R<sub>7</sub> (R<sub>7</sub> = 53 k) and C = 390 pF  $f_{C} = 7.55$  kHz or  $\omega_{C} = 47$  krad/sec

The application example in Figure 17a of a 320 MHz FM transmitter demonstrates the FM capabilities of the IC. A high value series resistor (100 k) to Pin 6 sets up the current source to drive the modulation section of the chip. Its value is dependent on the peak to peak level of the encoding data and the maximum desired frequency deviation. The data input is AC coupled with a large coupling capacitor which is selected for the modulating frequency. The component placements on the circuit side and ground side of the PC board are shown in Figures 28 and 29, respectively. Figure 18a illustrates the input data of a 10 kHz modulating signal at 1.6 Vp–p. Figures 18b and 18c depict the deviation and resulting modulation spectrum showing the carrier null at – 40 dBc. Figure 18d shows the unmodulated carrier power output at 3.5 dBm for  $V_{CC} = 3.0$  Vdc.

For voice applications using a dynamic or an electret microphone, an op amp is used to amplify the microphone's low level output. The microphone amplifier circuit is shown in Figure 19. Figure 17b shows an application example for NBFM audio or direct FSK in which the reference crystal oscillator is modulated.

### Figure 19. Microphone Amplifier



### **Local Oscillator Application**

To reduce internal loop noise, a relatively wide loop bandwidth is needed so that the loop tracks out or cancels the noise. This is emphasized to reduce inherent CCO and divider noise or noise produced by mechanical shock and environmental vibrations. In a local oscillator application the CCO and divider noise should be reduced by proper selection of the natural frequency of the loop. Additional low pass filtering of the output will likely be necessary to reduce the crystal sideband spurs to a minimal level.

### Figure 17a. 320 MHz MC13176D FM Transmitter



#### **NOTES:** 1.50 $\Omega$ coaxial balun, 2 inches long.

2. Pins 5, 10 and 15 are grounds and connnected to V<sub>EE</sub> which is the component's side ground plane.

These pins must be decoupled to V<sub>CC</sub>; decoupling capacitors should be placed as close as possible to the pins.

- 3. RFC<sub>1</sub> is 180 nH Coilcraft surface mount inductor or 190 nH Coilcraft 146–05J08.
- 4. Recommended source is a Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3-682.

5. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

# Figure 17b. 320 MHz NBFM Transmitter



**NOTES:** 1.50  $\Omega$  coaxial balun, 2 inches long.

2. Pins 5, 10 and 15 are grounds and connnected to VEE which is the component's side ground plane. These

- pins must be decoupled to V<sub>CC</sub>; decoupling capacitors should be placed as close as possible to the pins.
- 3. RFC<sub>1</sub> is 180 nH Coilcraft surface mount inductor.

4. RFC<sub>2</sub> and RFC<sub>3</sub> are high impedance crystal frequency of 10 MHz; 8.2  $\mu$ H molded inductor gives XL > 1000  $\Omega$ .

5. A single varactor like the MV2105 may be used whereby RFC<sub>2</sub> is not needed.

6. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

#### Figure 18a. Input Data Waveform



Figure 18c. Modulation Spectrum



### Reference Crystal Oscillator (Pins 8 and 9)

Selection of Proper Crystal: A crystal can operate in a number of mechanical modes. The lowest resonant frequency mode is its fundamental while higher order modes are called overtones. At each mechanical resonance, a crystal behaves like a RLC series–tuned circuit having a large inductor and a high Q. The inductor  $L_S$  is series resonance with a dynamic capacitor,  $C_S$  determined by the elasticity of the crystal lattice and a series resistance  $R_S$ , which accounts for the power dissipated in heating the crystal. This series RLC circuit is in parallel with a static capacitance,  $C_p$  which is created by the crystal block and by the metal plates and leads that make contact with it.

Figure 20 is the equivalent circuit for a crystal in a single resonant mode. It is assumed that other modes of resonance are so far off frequency that their effects are negligible.

Series resonant frequency, f<sub>S</sub> is given by;

and parallel resonant frequency, fp is given by;

$$f_p = f_s (1 + C_s / C_p)^{1/2}$$

#### Figure 18b. Frequency Deviation

-09.9 DBI	N INPUT LEVEL	72.0 ×V
	ERROR KHZ	+ 0.19
-15	Ū	+15
-42.5	DEV KHZ	+42.3
100	0	+100

Figure 18d. Unmodulated Carrier

unitum r		1 350	.000	nn2
03.5 DBM	INPUT	LEVEL	336,0	0 <b>.</b> .v
	ERRE	K KHZ	+ (	0.23
-15	ü			+15
0.14	DE:	KHZ	+1	0,17
-100	0		ATT	+100

Figure 20. Crystal Equivalent Circuit



the frequency separation at resonance is given by;

 $\Delta f = f_p - f_s = f_s [1 - (1 + C_s/C_p)^{1/2}]$ 

Usually  $f_p$  is less than 1% higher than  $f_s$ , and a crystal exhibits an extremely wide variation of the reactance with frequency between  $f_p$  and  $f_s$ . A crystal oscillator circuit is very stable with frequency. This high rate of change of impedance with frequency stabilizes the oscillator, because any significant change in oscillator frequency will cause a large phase shift in the feedback loop keeping the oscillator on frequency. Manufacturers specify crystal for either series or parallel resonant operation. The frequency for the parallel mode is calibrated with a specified shunt capacitance called a "load capacitance." The most common value is 30 to 32 pF. If the load capacitance is placed in series with the crystal, the equivalent circuit will be series resonance at the specified parallel–resonant frequency. Frequencies up to 20 MHz use parallel resonant crystal operating in the fundamental mode, while above 20 MHz to about 60 MHz, a series resonant crystal specified and calibrated for operation in the overtone mode is used.

### **Application Examples**

Two types of crystal oscillator circuits are used in the applications circuits: 1) fundamental mode common emitter Colpitts (Figures 1, 17a, 17b, and 21), and 2) third overtone impedance inversion Colpitts (also Figures 1 and 21).

The fundamental mode common emitter Colpitts uses a parallel resonant crystal calibrated with a 32 pf load capacitance. The capacitance values are chosen to provide excellent frequency stability and output power of > 500 mVp-p at Pin 9. In Figures 1 and 21, the fundamental mode reference oscillator is fixed tuned relying on the repeatability of the crystal and passive network to maintain the frequency, while in the circuit shown in Figure 17, the oscillator frequency can be adjusted with the variable inductor for the precise operating frequency.

The third overtone impedance inversion Colpitts uses a series resonance crystal with a 25 ppm tolerance. In the application examples (Figures 1 and 21), the reference oscillator operates with the third overtone crystal at 40.0000 MHz. Thus, the MC13175 is operated at 320 MHz ( $f_0/8$  = crystal; 320/8 = 40.0000 MHz. The resistor across the crystal ensures that the crystal will operate in the series resonant mode. A tuneable inductor is used to adjust the oscillation frequency; it forms a parallel resonant circuit with the series and parallel combination of the external capacitors forming the divider and feedback network and the base–emitter capacitance of the device. If the crystal is shorted, the reference oscillator should free–run at the frequency dictated by the parallel resonant LC network.

The reference oscillator can be operated as high as 60 MHz with a third overtone crystal. Therefore, it is possible to use the MC13175 up to at least 480 MHz and the MC13176 up to 950 MHz (based on the maximum capability of the divider network).

## Enable (Pin 11)

The enabling resistor at Pin 11 is calculated by: Reg. enable =  $V_{CC} - 1.0 \text{ Vdc/I}_{reg. enable}$  From Figure 4, I<sub>reg. enable</sub> is chosen to be 75  $\mu$ A. So, for a V<sub>CC</sub> = 3.0 Vdc R<sub>reg. enable</sub> = 26.6 k $\Omega$ , a standard value 27 k $\Omega$  resistor is adequate.

### Layout Considerations

Supply (Pin 12): In the PCB layout, the V<sub>CC</sub> trace must be kept as wide as possible to minimize inductive reactance along the trace; it is best that  $V_{CC}$  (RF ground) completely fills around the surface mounted components and interconnect traces on the circuit side of the board. This technique is demonstrated in the evaluation PC board.

### **Battery/Selection/Lithium Types**

The device may be operated from a 3.0 V lithium battery. Selection of a suitable battery is important. Because one of the major problems for long life battery powered equipment is oxidation of the battery terminals, a battery mounted in a clip-in socket is not advised. The battery leads or contact post should be isolated from the air to eliminate oxide build-up. The battery should have PC board mounting tabs which can be soldered to the PCB. Consideration should be given for the peak current capability of the battery. Lithium batteries have current handling capabilities based on the composition of the lithium compound, construction and the battery size. A 1300 mA/hr rating can be achieved in the cylindrical cell battery. The Rayovac CR2/3A lithium-manganese dioxide battery is a crimp sealed, spiral wound 3.0 Vdc, 1300 mA/hr cylindrical cell with PC board mounting tabs. It is an excellent choice based on capacity and size (1.358" long by 0.665" in diameter).

### Differential Output (Pins 13, 14)

The availability of micro–coaxial cable and small baluns in surface mount and radial–leaded components allows for simple interface to the output ports. A loop antenna may be directly connected with bias via RFC or 50  $\Omega$  resistors. Antenna configuration will vary depending on the space available and the frequency of operation.

## AM Modulation (Pin 16)

**Amplitude Shift Key:** The MC13175 and MC13176 are designed to accommodate Amplitude Shift Keying (ASK). ASK modulation is a form of digital modulation corresponding to AM. The amplitude of the carrier is switched between two or more values in response to the PCM code. For the binary case, the usual choice is On–Off Keying (often abbreviated OOK). The resultant amplitude modulated waveform consists of RF pulses called marks, representing binary 1 and spaces representing binary 0.

### Figure 21. ASK 320 MHz Application Circuit



- NOTES: 1.50  $\Omega$  coaxial balun, 1/10 wavelength line (1.5") provides the best match to a 50  $\Omega$  load.
  - 2. Pins 5, 10 and 15 are ground and connnected to V<sub>EE</sub> which is the component/DC ground plane side of PCB. These pins must be decoupled to V<sub>CC</sub>; decoupling capacitors should be placed as close as possible to the pins.
  - The crystal oscillator circuit may be adjusted for frequency with the variable inductor (MC13175); 1.0 k resistor shunting the crystal prevents it from oscillating in the fundamental mode. Recommended source is Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3–821.
- 4. The On–Off keyed signal turns the output of the transmitter off and on with TTL level pulses through R<sub>mod</sub> at Pin 16. The "On" power and I<sub>CC</sub> is set by the resistor which sets I<sub>mod</sub> = VTTL 0.8 / R<sub>mod</sub>. (see Figure 23).
- 5. S1 simulates an enable gate pulse from a microprocessor which will enable the transmitter. (see Figure 4 to determine precise value of the enabling resistor based on the potential of the gate pulse and the desired enable.)

Figure 21 shows a typical application in which the output power has been reduced for linearity and current drain. The current draw on the device is 16 mA I<sub>CC</sub> (average) and -22.5 dBm (average power output) using a 10 kHz modulating rate for the on–off keying. This equates to 20 mA and -2.3 dBm "On", 13 mA and -41 dBm "Off". In Figure 22a, the device's modulating waveform and encoded carrier

are displayed. The crystal oscillator enable time is needed to set the acquisition timing. It takes typically 4.0 msec to reach full magnitude of the oscillator waveform (see Figure 22b, Oscillator Waveform, at Pin 8). A square waveform of 3.0 V peak with a period that is greater than the oscillator enable time is applied to the Enable (Pin 11).

### Figure 22a. ASK Input Waveform and Modulated Carrier







Figure 23. Power Output versus Modulation Current



### Analog AM

In analog AM applications, the output amplifier's linearity must be carefully considered. Figure 23 is a plot of Power Output versus Modulation Current at 320 MHz, 3.0 Vdc. In order to achieve a linear encoding of the modulating sinusoidal waveform on the carrier, the modulating signal must amplitude modulate the carrier in the linear portion of its power output response. When using a sinewave modulating signal, the signal rides on a positive DC offset called V<sub>mod</sub> which sets a static (modulation off) modulation current, I<sub>mod</sub>. I<sub>mod</sub> controls the power output of the IC. As the modulating signal moves around this static bias point the modulating current varies causing power output to vary or to be AM modulated. When the IC is operated at modulation current levels greater than 2.0 mAdc the differential output stage starts to saturate.

In the design example, shown in Figure 24, the operating point is selected as a tradeoff between average power output and quality of the AM.

For V<sub>CC</sub> = 3.0 Vdc; I<sub>CC</sub> = 18.5 mA and I<sub>mod</sub> = 0.5 mAdc and a static DC offset of 1.04 Vdc, the circuit shown in Figure 24 completes the design. Figures 25a, 25b and 25c show the results of -6.9 dBm output power and 100% modulation by the 10 kHz and 1.0 MHz modulating sinewave signals. The amplitude of the input signals is approximately 800 mVp–p.

Where  $R_{mod} = (V_{CC} - 1.04 \text{ Vdc})/0.5 \text{ mA} = 3.92 \text{ k}$ , use a standard value resistor of 3.9 k.

### Figure 24. Analog AM Transmitter





## Figure 25a. Power Output of Unmodulated Carrier

Figure 25b. Input Signal and AM Modulated Carrier for f<sub>mod</sub> = 10 kHz



Figure 25c. Input Signal and AM Modulated Carrier for f<sub>mod</sub> = 1.0 MHz



Figure 26. Circuit Side View of MC1317XD



Figure 27. Ground Side View



Figure 28. Surface Mounted Components Placement (on Circuit Side)



Figure 29. Radial Leaded Components Placement (on Ground Side)



# **Tape and Reel Options**

# In Brief . . .

Motorola offers the convenience of Tape and Reel packaging for our growing family of standard integrated circuit products. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

	Page
Tape and Reel Configurations	12-2
Tape and Reel Information Table	12–4
Analog MPQ Table	12–5



**Mechanical Polarization** 





User Direction of Feed











# **Tape and Reel Information Table**

Package	Tape Width (mm)	Devices <sup>(1)</sup> per Reel	Reel Size (inch)	Device Suffix
SO8, SOP8 SO14 SO16	12 16 16	2,500 2,500 2,500	13 13 13	R2 R2 R2
SO-16L, SO-8+8L WIDE SO-20L WIDE SO-24L WIDE SO-28L WIDE SO-28L WIDE	16 24 24 24 32	1,000 1,000 1,000 1,000 1,000	13 13 13 13 13 13	R2 R2 R2 R2 R3
Micro-8	12	2,500	13	R2
PLCC-20 PLCC-28 PLCC-44	16 24 32	1,000 500 500	13 13 13	R2 R2 R2
PLCC-52 PLCC-68 PLCC-84	32 44 44	500 250 250	13 13 13	R2 R2 R2
TO-226AA (TO-92) <sup>(2)</sup>	18	2,000	13	RA, RE, RP, or RM (Ammo Pack) only
DPAK	16	2,500	13	RK
D <sup>2</sup> PAK	24	800	13	R4
SOT-23 (5 Pin)	8	3,000	7	TR
SOT-89 (3/5 Pin)	12	1,000	7	T1

(1) Minimum order quantity is 1 reel. Distributors/OEM customers may break lots or reels at their option, however broken reels may not be returned. (2) Integrated circuits in TO–226AA packages are available in Styes A and E only, with optional "Ammo Pack" (Suffix RP or RM). The RA and RP configurations are preferred. For ordering information please contact your local Motorola Semiconductor Sales Office.

# Analog MPQ Table

# Tape/Reel and Ammo Pack

Package Type	Package Code	MPQ		
PLCC	-	-		
Case 775	0802	1000/reel		
Case 776	0804	500/reel		
Case 777	0801	500/reel		
SOIC				
Case 751	0095	2500/reel		
Case 751A	0096	2500/reel		
Case 751B	0097	2500/reel		
Case 751G	2003	1000/reel		
Case 751D	2005	1000/reel		
Case 751E	2008	1000/reel		
Case 751F	2009	1000/reel		
Micro-8				
Case 846A	-	2500/reel		
TO-92				
Case 29	0031	2000/reel		
Case 29	0031	2000/Ammo Pack		
DPAK	-			
Case 369A	-	2500/reel		
D <sup>2</sup> PAK				
Case 936	-	800/reel		
SOT–23 (5 Pin)				
Case 1212	-	3000/reel		
SOT–89 (3 Pin)				
Case 1213	_	1000/reel		
SOT–89 (5 Pin)				
Case 1214	-	1000/reel		

# **Packaging Information**

# In Brief ...

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(TA)} = \frac{T_{J(max)} - T_{A}}{R_{\theta}JA(Typ)}$$

where:

- PD(TA) = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.
- T<sub>J(max)</sub> = Maximum operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for T<sub>J(max)</sub> information.
  - T<sub>A</sub> = Maximum desired operating Ambient Temperature
- R<sub>0JA(Typ)</sub> = Typical Thermal Resistance Junction-to-Ambient

# **Case Outline Dimensions**



















![](_page_33_Figure_0.jpeg)

![](_page_34_Figure_0.jpeg)

![](_page_35_Figure_0.jpeg)

![](_page_36_Figure_0.jpeg)

![](_page_37_Figure_0.jpeg)

![](_page_38_Figure_0.jpeg)

**FB SUFFIX** CASE 824E-02 **Plastic Package** (QFP) **ISSUE A** 

![](_page_39_Picture_1.jpeg)

![](_page_39_Figure_2.jpeg)

![](_page_39_Figure_3.jpeg)

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
   DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD

- LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE. 4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-. 5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-. 6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
- DETERMINED AT DATUM PLANE –H–. 7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.90	10.10	0.390	0.398
В	9.90	10.10	0.390	0.398
С	2.00	2.21	0.079	0.087
D	0.30	0.45	0.0118	0.0177
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80	BSC	0.031	BSC
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
M	5°	10 °	5°	10°
S	12.95	13.45	0.510	0.530
V	12.95	13.45	0.510	0.530
W	0.000	0.210	0.000	0.008
Y	5°	10 °	5°	10°
A1	0.450 REF		0.018	REF
B1	0.130	0.170	0.005	0.007
C1	1.600	REF	0.063	REF
R1	0.130	0.300	0.005	0.012
R2	0.130	0.300	0.005	0.012
θ1	5°	10 °	5°	10°
θ2	00	7 °	0°	7°

![](_page_40_Figure_0.jpeg)

![](_page_41_Figure_0.jpeg)

![](_page_42_Figure_0.jpeg)

![](_page_43_Figure_0.jpeg)

![](_page_44_Figure_0.jpeg)

![](_page_45_Figure_0.jpeg)

![](_page_46_Figure_0.jpeg)

![](_page_47_Figure_0.jpeg)

![](_page_48_Figure_0.jpeg)

![](_page_49_Figure_0.jpeg)

![](_page_50_Figure_0.jpeg)

![](_page_50_Picture_1.jpeg)

![](_page_50_Figure_2.jpeg)

NOTES:

1 DIMENSIONING AND TOLERANCING PER ANSI

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
   CONTROLLING DIMENSION: MILLIMETER.
   DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- (U.UU6) PER SIDE. 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 0.25 (0.010) PER SIDE. 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. 6 TERMINAL NUMBERS ARE SHOWN FOR DEFEDENCE ONLY
- 7 ETERMINAL NOMBER'S ARE SHOWN FOR REFERENCE ONLY.
  7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
К	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
M	0.0	8°	00	8°

![](_page_51_Picture_1.jpeg)

![](_page_51_Figure_2.jpeg)

NOTES:

- IOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. DIMENSION P. DOES NOT INCLUDE INTERLEAD.
- (0.000) PEX SIDE. 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMIBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. 6. TERMINAL NUMBERS ARE SHOWN FOR DEFENSION ON MALE AND A DAMIBARS ARE SHOWN FOR
- REFERENCE ONLY.
  DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	7.70	7.90	0.303	0.311
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8°	0 °	8 °

![](_page_52_Figure_0.jpeg)

![](_page_53_Figure_0.jpeg)

![](_page_54_Figure_0.jpeg)

![](_page_55_Figure_0.jpeg)