FAIRCHILD™

June 2015

LMV321 / LMV358 / LMV324 General-Purpose, Low Voltage, Rail-to-Rail Output Amplifiers

Features at +2.7V

- 80 µA Supply Current per Channel
- 1.2 MHz Gain Bandwidth Product
- Output Voltage Range: 0.01 V to 2.69 V
- Input Voltage Range: -0.25 V to +1.5 V
- 1.5 V/µs Slew Rate
- LMV321 Directly Replaces Other Industry Standard LMV321 Amplifiers: Available in SC70-5 and SOT23-5 Packages
- LMV358 Directly Replaces Other Industry Standard LMV358 Amplifiers: Available in MSOP-8 and SOIC-8 Packages
- LMV324 Directly Replaces Other Industry Standard LMV324 Amplifiers: Available in SOIC-14 Packages
- Fully Specified at +2.7 V and +5 V Supplies
- Operating Temperature Range: -40°C to +125°C

Applications

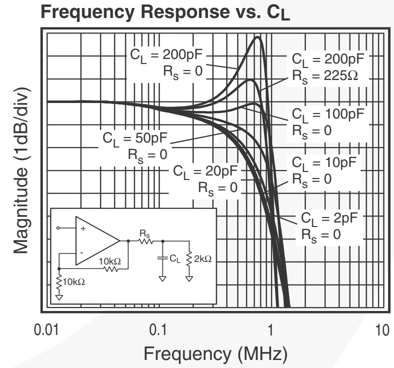
- Low Cost General-Purpose Applications
- Cellular Phones
- Personal Data Assistants
- A/D Buffer
- DSP Interface
- Smart Card Readers
- Portable Test Instruments
- Keyless Entry
- Infrared Receivers for Remote Controls
- Telephone Systems
- Audio Applications
- Digital Still Cameras
- Hard Disk Drives
- MP3 Players

Description

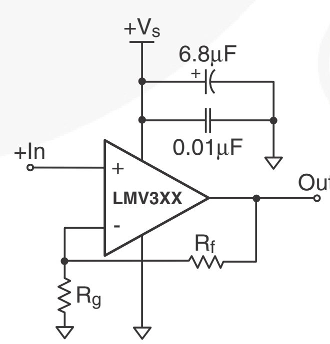
The LMV321 (single), LMV358 (dual), and LMV324 (quad) are a low cost, voltage feedback amplifiers that consume only 80 µA of supply current per amplifier. The LMV3XX family is designed to operate from 2.7 V (±1.35 V) to 5.5 V (±2.75 V) supplies. The common mode voltage range extends below the negative rail and the output provides rail-to-rail performance.

The LMV3XX family is designed on a CMOS process and provides 1.2 MHz of bandwidth and 1.5 V/µs of slew rate at a low supply voltage of 2.7 V. The combination of low power, rail-to-rail performance, low voltage operation, and tiny pack-age options make the LMV3XX family well suited for use in personal electronics equipment such as cellular handsets, pagers, PDAs, and other battery powered applications.

Frequency Response vs. C_L



Typical Application



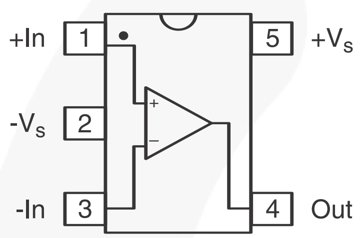
Ordering Information

Product Number	Package	Packing Method	Operating Temperature
LMV321AP5X	SC70 5L	Tape and Reel, 3000pcs	-40 to +125°C
LMV321AS5X	SOT-23 5L	Tape and Reel, 3000pcs	
LMV358AM8X	SOIC 8L (Narrow)	Tape and Reel, 2500pcs	
LMV358AMU8X	MSOP 8L	Tape and Reel, 3000pcs	
LMV324AM14X	SOIC 14L	Tape and Reel, 2500pcs	

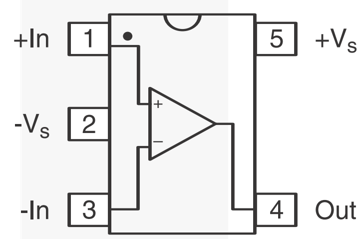
Pin Assignments

LMV321

SOT23-5

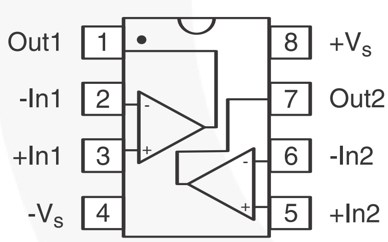


SC70-5

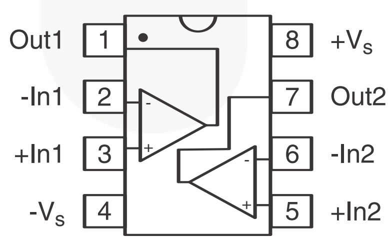


LMV358

SOIC-8

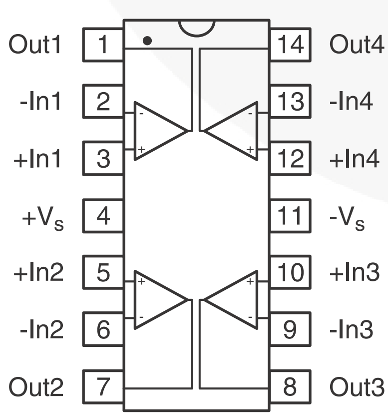


MSOP-8



LMV324

SOIC-14



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Min.	Max.	Unit
Supply Voltage	0	+6	V
Maximum Junction Temperature	-	+175	°C
Storage Temperature Range	-65	+150	°C
Lead Temperature, 10 Seconds	-	+260	°C
Input Voltage Range	$-V_S$ -0.5	$+V_S$ +0.5	V

Recommended Operating Conditions

Parameter	Min.	Max.	Unit
Operating Temperature Range	-40	+125	°C
Power Supply Operating Range	2.5	5.5	V

Package Thermal Resistance

Package	θ_{JA}	Unit
5 Lead SC70	331.4	°C/W
5 Lead SOT23	256	°C/W
8 Lead SOIC	152	°C/W
8 Lead MSOP	206	°C/W
14 Lead SOIC	88	°C/W

Electrical Specifications

T_C = 25°C, V_S = +2.7 V, G = 2, R_L = 10 kΩ to V_S/2, R_f = 10 kΩ, $V_{O(DC)}$ = V_{CC}/2, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Unit
AC Performance						
Gain Bandwidth Product		C_L= 50 pF, R_L= 2 kΩ to V_S/2		1.2		MHz
Phase Margin				52		deg
Gain Margin				17		dB
Slew Rate		V_O = 1V_{PP}		1.5		V/µs
Input Voltage Noise		>50 kHz		36		nV/√Hz
Crosstalk	LMV358	100 kHz		91		dB
	LMV324	100 kHz		80		
DC Performance						
Input Offset Voltage(1)				1.7	7.0	mV
Average Drift				8		µV/°C
Input Bias Current(2)				<1		nA
Input Offset Current(2)				<1		nA
Power Supply Rejection Ratio(1)		DC	50	65		dB
Supply Current (Per Channel)(1)				80	120	µA
Input Characteristics						
Input Common Mode Voltage Range(1)		LO	0	-0.25		V
		HI		1.5	1.3	
Common Mode Rejection Ratio(1)			50	70		dB
Output Characteristics						
Output Voltage Swing		R_L= 10 kΩ to V_S/2; LO(1)		0.01	0.10	V
		R_L= 10 kΩ to V_S/2; HI(1)	2.60	2.69		

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes:
1. Guaranteed by testing or statistical analysis at +25°C.
2. +IN and -IN are gates to CMOS transistors with typical input bias current of <1 nA. CMOS leakage is too small to practically measure.

Electrical Specifications (Continued)

T_C = 25°C, V_S = +5 V, G = 2, R_L = 10 kΩ to V_S/2, R_f = 10 kΩ, $V_{O(DC)}$ = V_{CC}/2, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Unit
AC Performance						
Gain Bandwidth Product		C_L= 50 pF, R_L= 2 kΩ to V_S/2		1.4		MHz
Phase Margin				73		deg
Gain Margin				12		dB
Slew Rate				1.5		V/µs
Input Voltage Noise		>50 kHz		33		nV/√Hz
Crosstalk	LMV358	100 kHz		91		dB
	LMV324	100 kHz		80		dB
DC Performance						
Input Offset Voltage(3)				1	7	mV
Average Drift				6		µV/°C
Input Bias Current(4)				<1		nA
Input Offset Current(4)				<1		nA
Power Supply Rejection Ratio(3)		DC	50	65		dB
Open Loop Gain(3)			50	70		dB
Supply Current (Per Channel)(3)				100	150	µA
Input Characteristics						
Input Common Mode Voltage Range(3)		LO	0	-0.4		V
		HI		3.8	3.6	V
Common Mode Rejection Ratio(3)			50	75		dB
Output Characteristics						
Output Voltage Swing		R_L= 2 kΩ to V_S/2; LO/HI		0.036 to 4.950		V
		R_L= 10 kΩ to V_S/2; LO(3)		0.013	0.100	V
		R_L= 10 kΩ to V_S/2; HI(3)	4.90	4.98		V
Short Circuit Output Current(3)		Sourcing; V_O = 0 V	5	+34		mA
		Sinking; V_O = 5 V	10	-23		mA

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

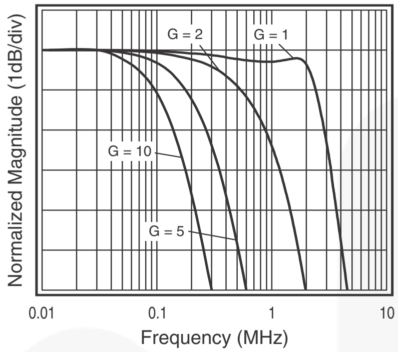
Notes:

3. Guaranteed by testing or statistical analysis at +25°C.
4. +IN and -IN are gates to CMOS transistors with typical input bias current of <1 nA. CMOS leakage is too small to practically measure.

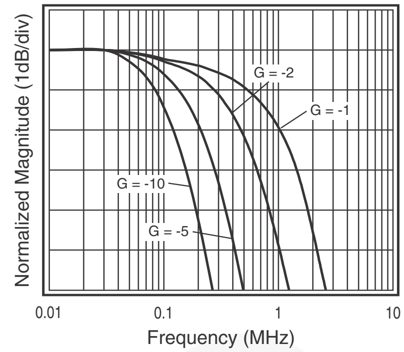
Typical Operating Characteristics

$T_C = 25°C$, $V_S = +5$ V, G = 2, $R_L = 10$ kΩ to $V_S/2$, $R_f = 10$ kΩ, $V_{O(DC)} = V_{CC}/2$, unless otherwise noted.

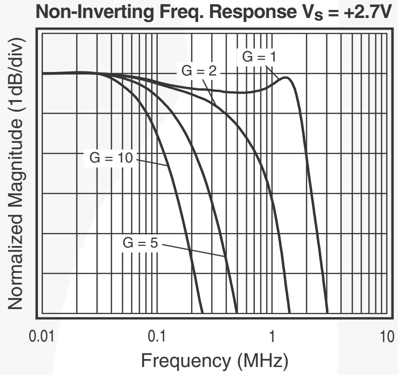
Non-Inverting Freq. Response V_S = +5V



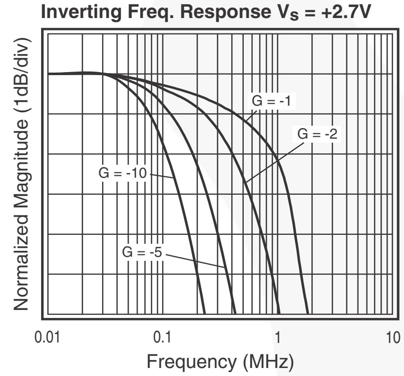
Inverting Frequency Response V_S = +5V



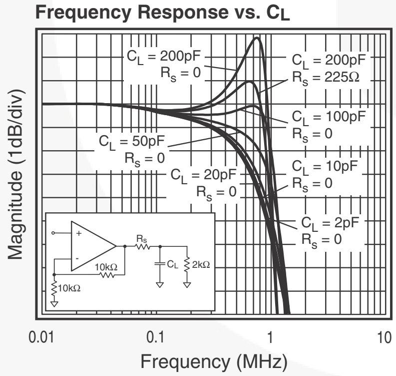
Non-Inverting Freq. Response V_S = +2.7V



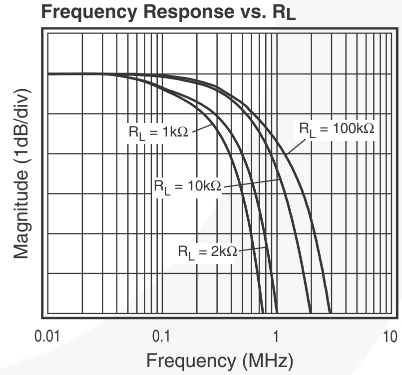
Inverting Freq. Response V_S = +2.7V



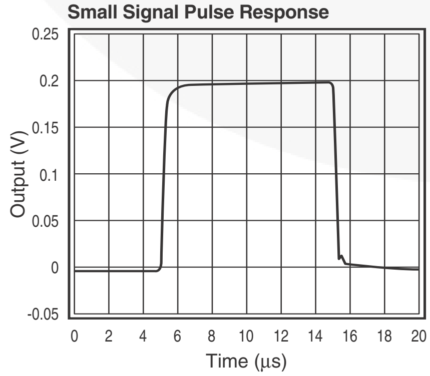
Frequency Response vs. C_L



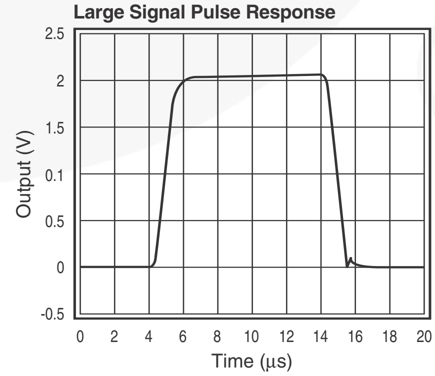
Frequency Response vs. R_L



Small Signal Pulse Response

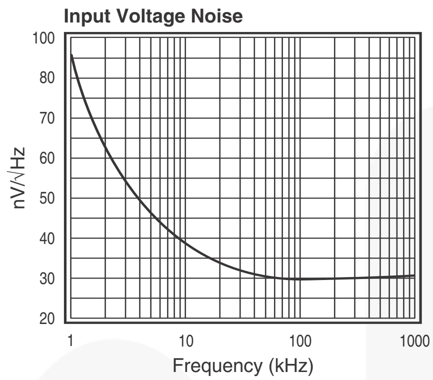


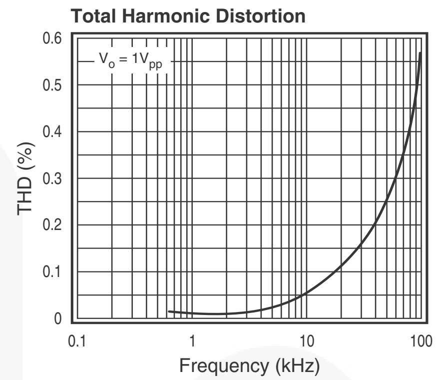
Large Signal Pulse Response

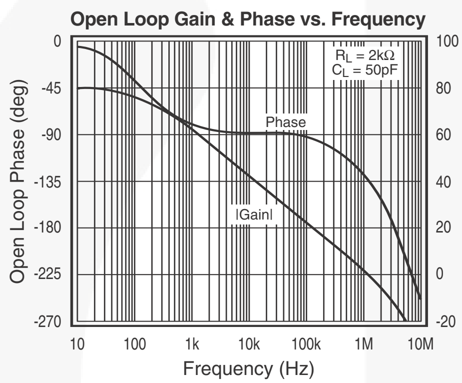


Typical Operating Characteristics (Continued)

T_C = 25°C, V_S = +5 V, G = 2, R_L = 10 kΩ to V_S/2, R_f = 10 kΩ, $V_{O(DC)}$ = V_{CC}/2, unless otherwise noted.







Application Information

General Description

The LMV3XX family are single supply, general-purpose, voltage-feedback amplifiers that are pin-for-pin compatible and drop in replacements with other industry standard LMV321, LMV358, and LMV324 amplifiers. The LMV3XX family is fabricated on a CMOS process, features a rail-to-rail output, and is unity gain stable.

The typical non-inverting circuit schematic is shown in Figure1.

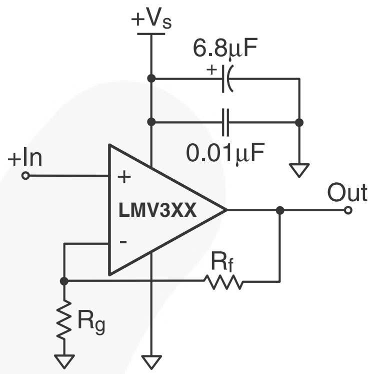


Figure 1. Typical Non-inverting configuration

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, some performance degradation will occur. If the maximum junction temperature exceeds 175°C for an extended time, device failure may occur.

Driving Capacitive Loads

The ***Frequency Response vs. C_L*** plot on page 4, illustrates the response of the LMV3XX family. A small series resistance (R_S) at the output of the amplifier, illustrated in Figure 2, will improve stability and settling performance. R_s values in the ***Frequency Response vs. C_L*** plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger R_S. As the plot indicates, the LMV3XX family can easily drive a 200 pF capacitive load without a series resistance. For comparison, the plot also shows the LMV321 driving a 200 pF load with a 225 Ω series resistance.

Driving a capacitive load introduces phase-lag into the output signal, which reduces phase margin in the amplifier. The unity gain follower is the most sensitive configuration. In a unity gain follower configuration, the LMV3XX family requires a 450 Ω series resistor to drive a 200 pF load. The response is illustrated in Figure 3.

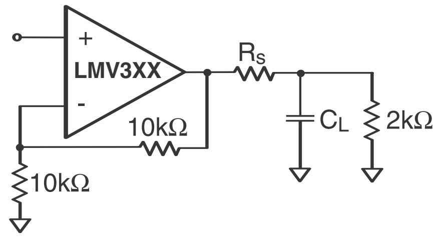


Figure 2. Typical Topology for driving a capacitive load

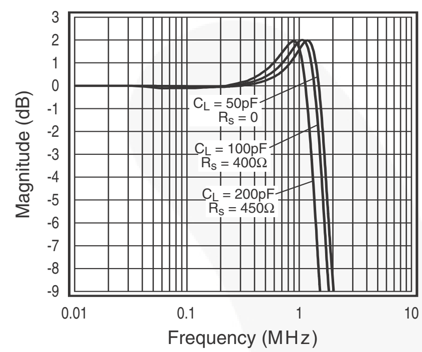


Figure 3. Frequency Response vs. C_L for unity gain configuration

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8 µF and 0.01 µF ceramic capacitors
- Place the 6.8 µF capacitor within 0.75 inches of the power pin
- Place the 0.01 µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts shown in Figure 5 on page 8 for more information.

Evaluation Board Information

The following evaluation boards are NOT available any more but their Schematic & Layout information will be useful for references to aid in the testing and layout of this device.

Evaluation board schematics and layouts are shown in Figures 4 and 5.

Eval Bd	Description	Products
KEB013	Single Channel, Dual Supply, SOT23-5 for Buffer-Style Pinout	LMV321AS5X
KEB014	Single Channel, Dual Supply, SC70-5 for Buffer-Style Pinout	LMV321AP5X
KEB006	Dual Channel, Dual Supply, 8 Lead SOIC	LMV358AM8X
KEB010	Dual Channel, Dual Supply, 8 Lead MSOP	LMV358AMU8X
KEB018	Quad Channel, Dual Supply, 14 Lead SOIC	LMV324AM14X

Evaluation Board Schematic Diagrams

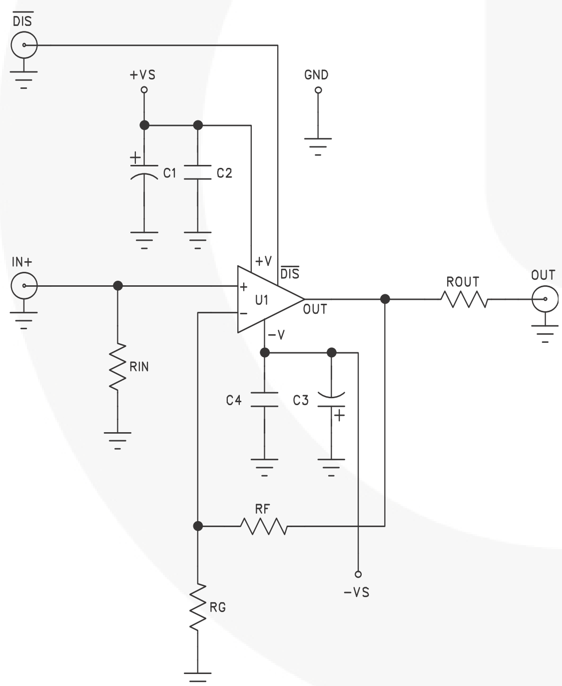


Figure 4a. LMV321 KEB013 schematic

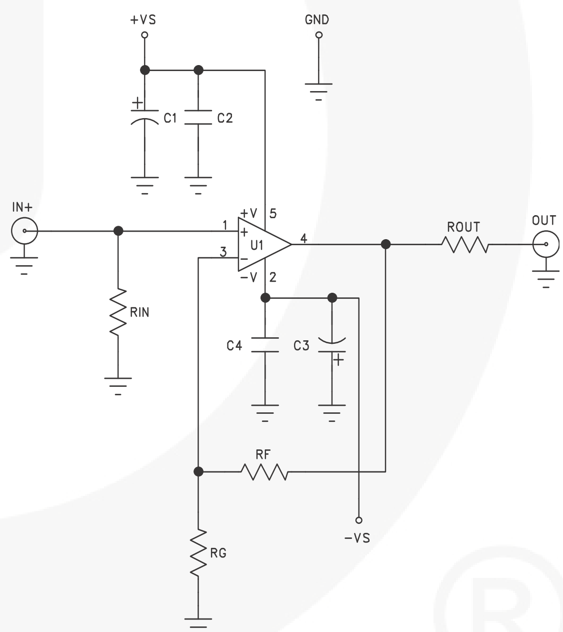


Figure 4b. LMV321 KEB014 schematic

Evaluation Board Schematic Diagrams (Continued)

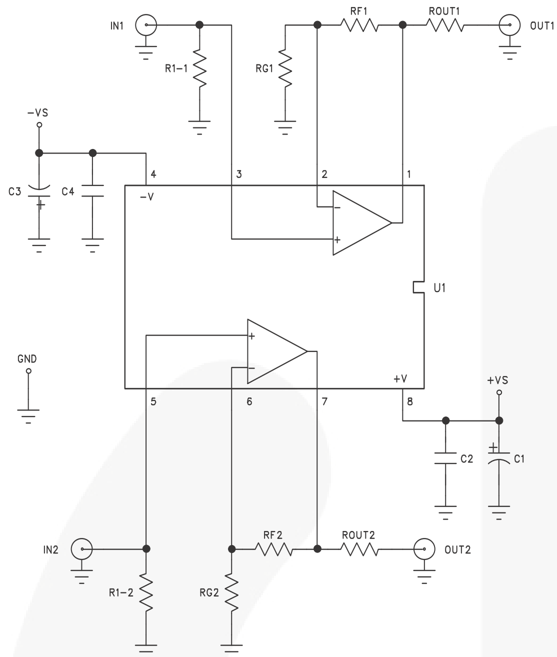


Figure 4c. LMV358 KEB006/KEB010 schematic

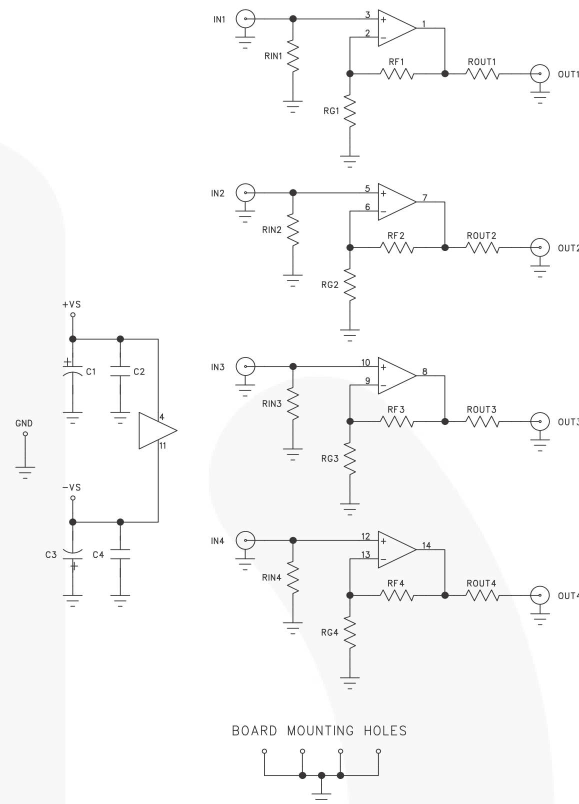


Figure 4d. LMV324 KEB018 schematic

LMV321 Evaluation Board Layout

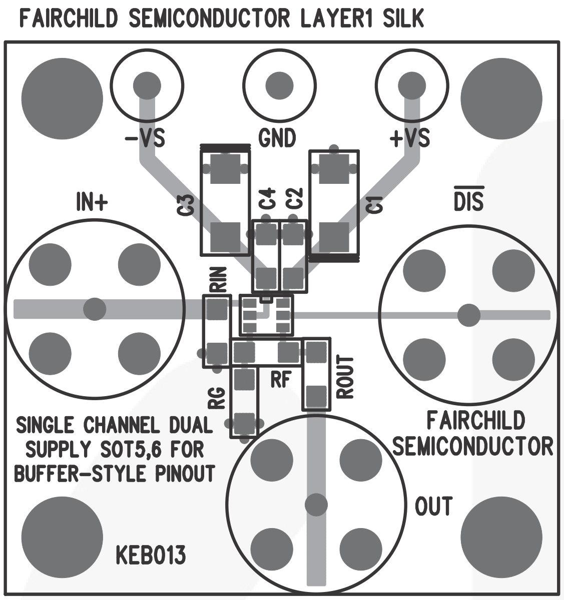


Figure 5a. KEB013 (top side)

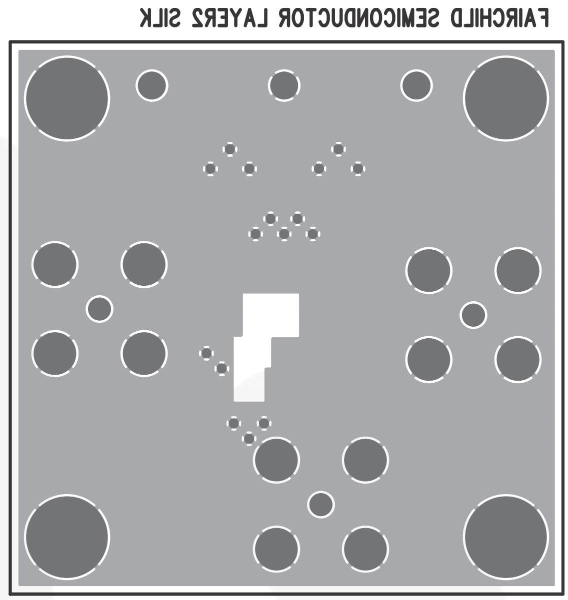


Figure 5b. KEB013 (bottom side)

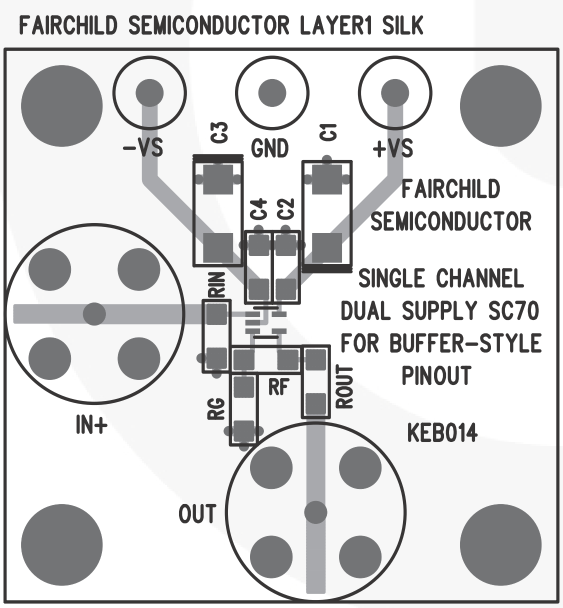


Figure 5c. KEB014 (top side)

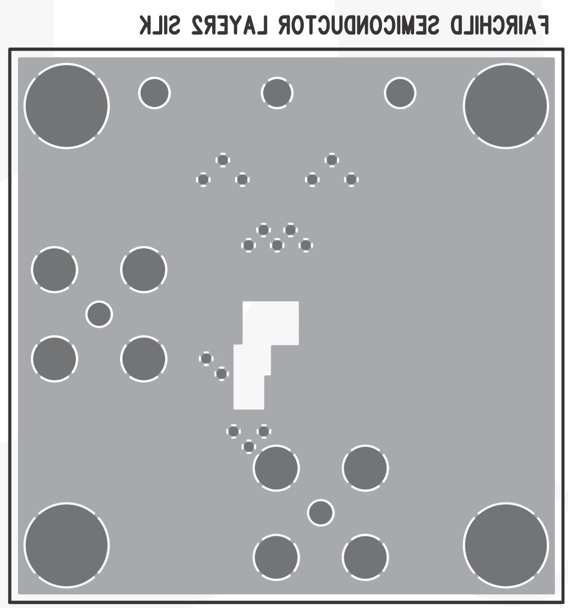


Figure 5d. KEB014 (bottom side)

LMV358 Evaluation Board Layout

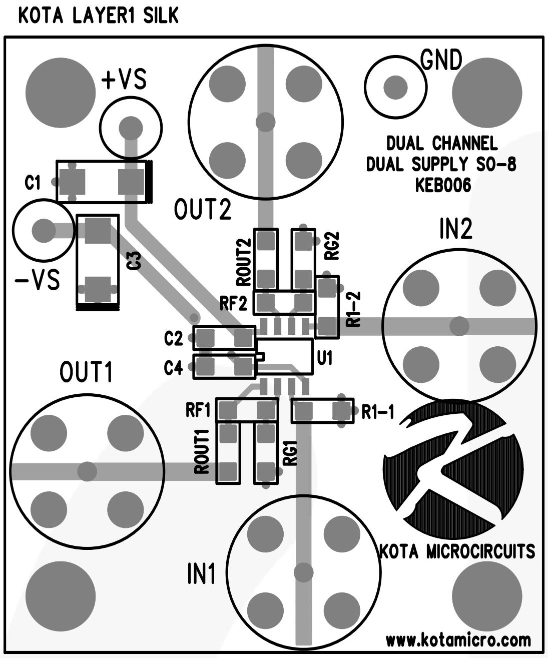


Figure 5e. KEB006 (top side)

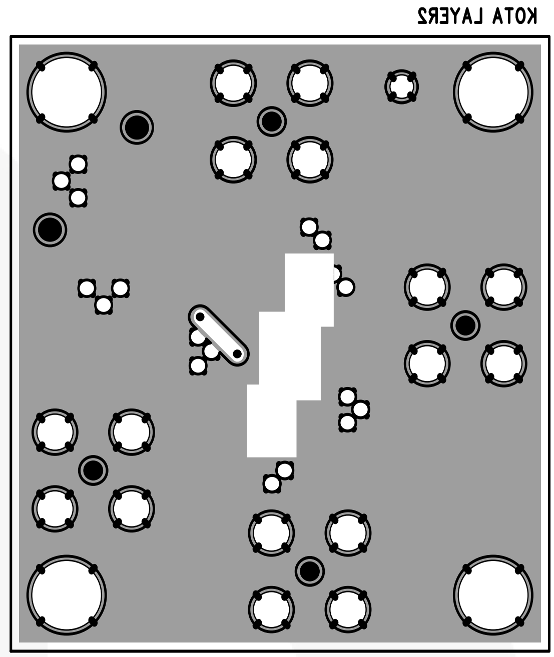


Figure 5f. KEB006 (bottom side)

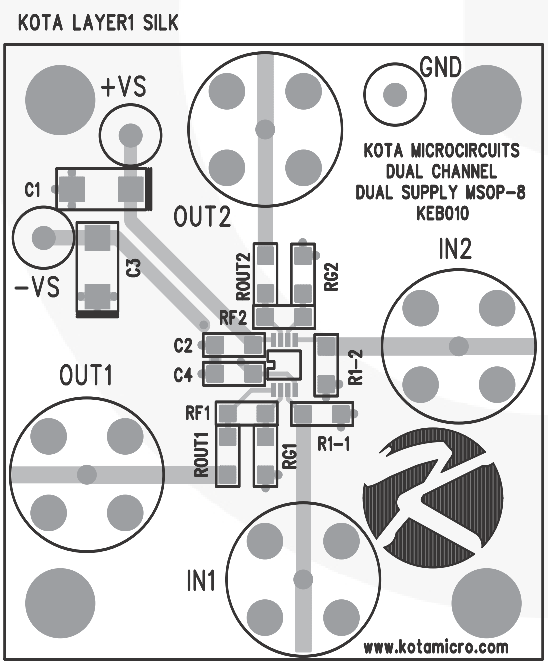


Figure 5g. KEB010 (top side)

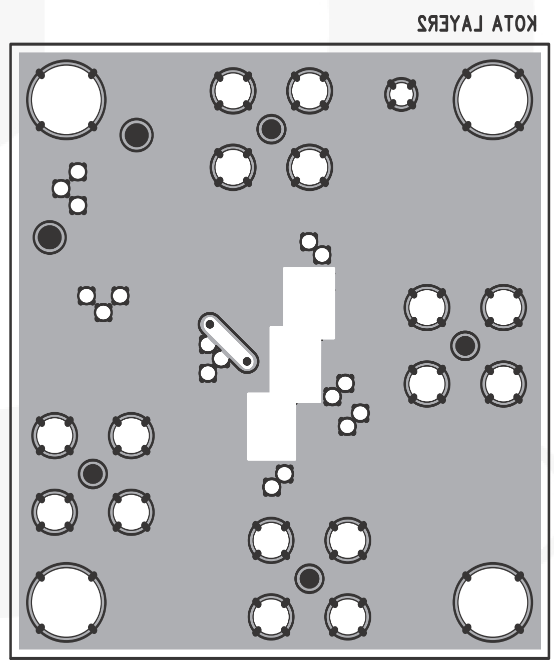


Figure 5h. KEB010 (bottom side)

LMV324 Evaluation Board Layout

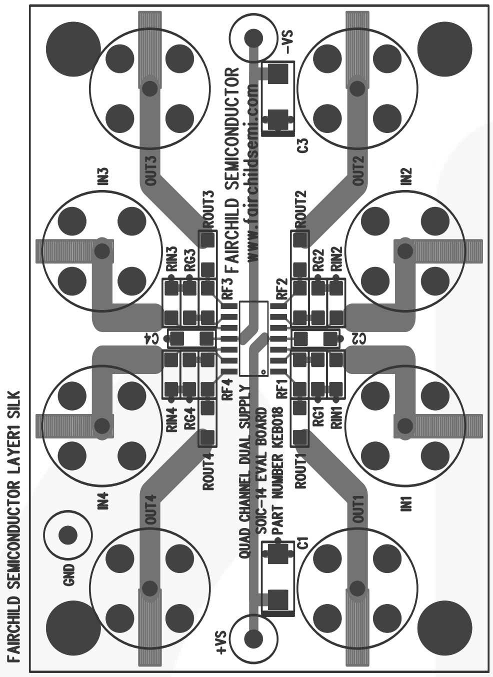


Figure 5i. KEB018 (top side)

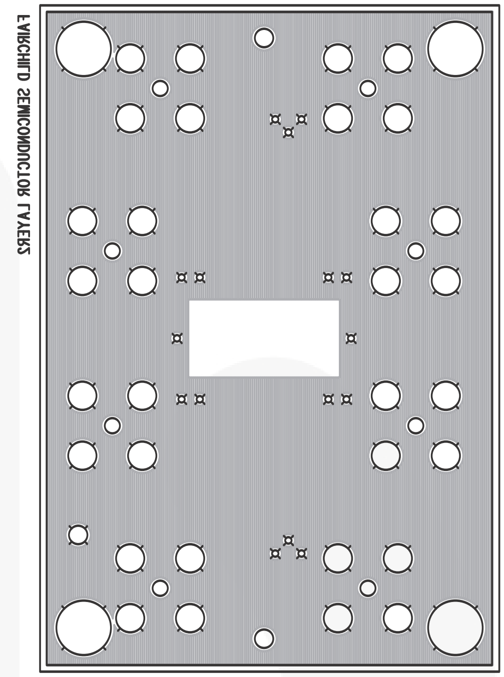
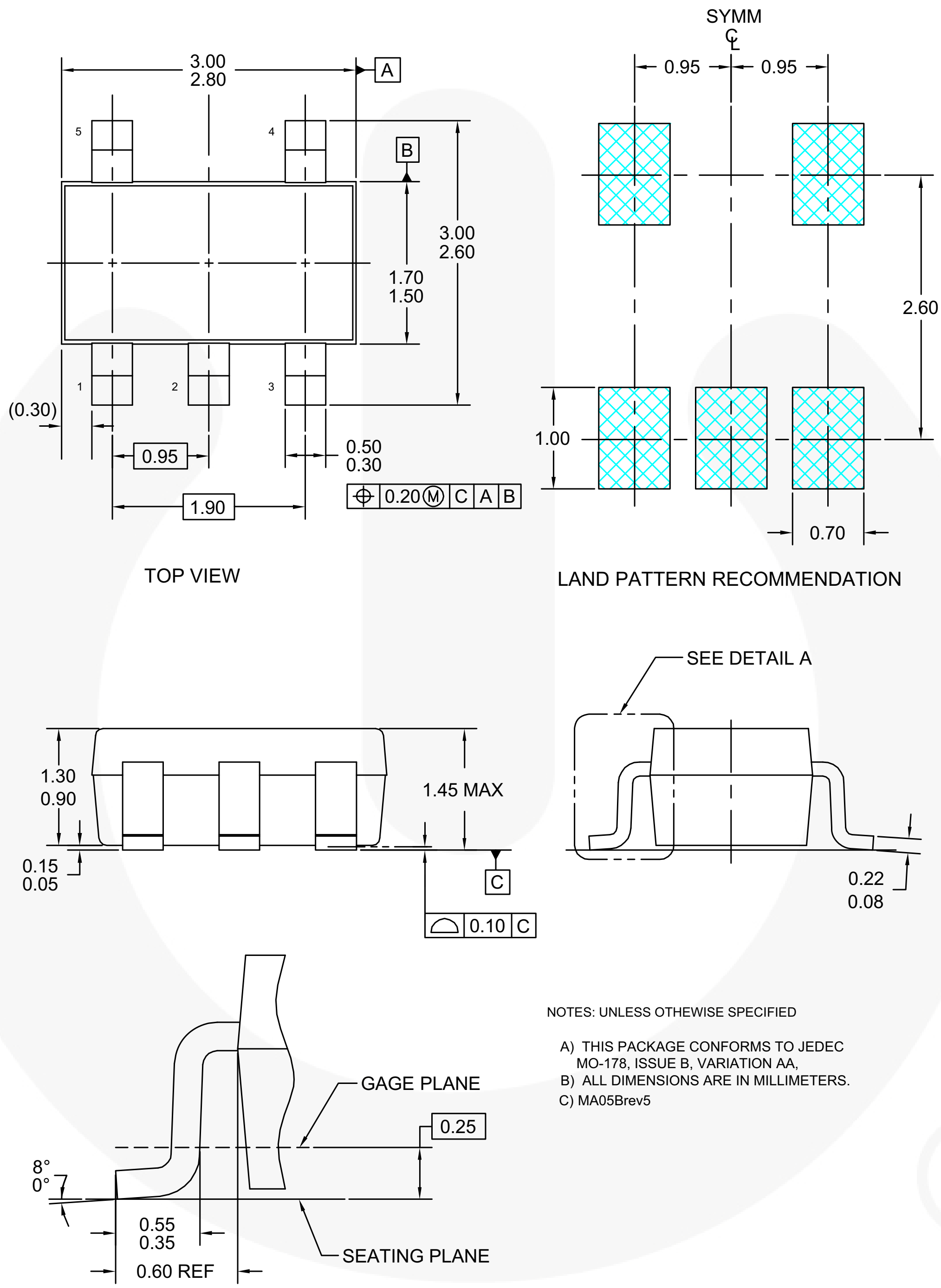


Figure 5j. KEB018 (bottom side)

Physical Dimensions



NOTES: UNLESS OTHEWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) MA05Brev5

Figure 6. 5-LEAD, SOT-23, JEDEC MO-178, 1.6MM

Physical Dimensions (Continued)

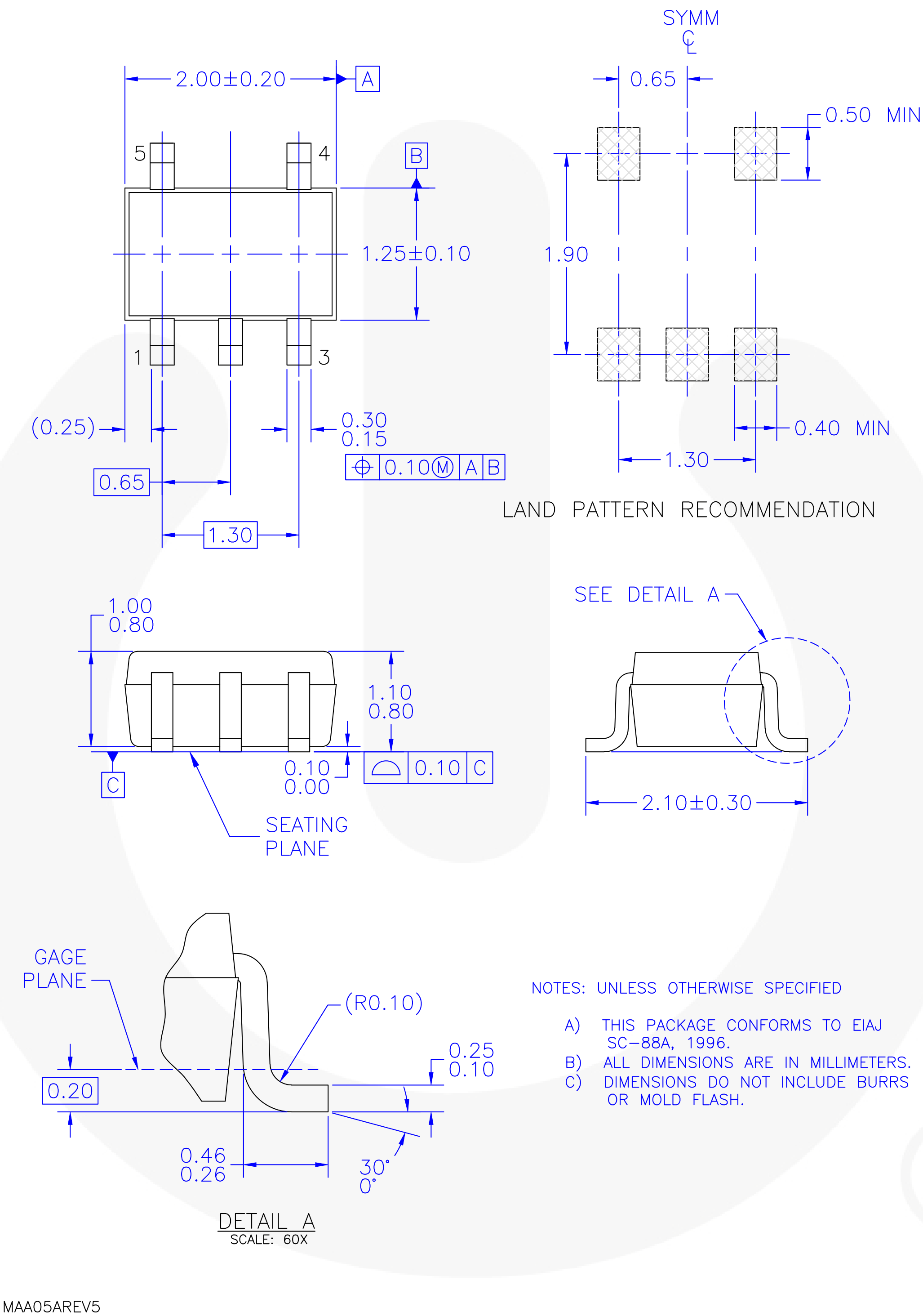
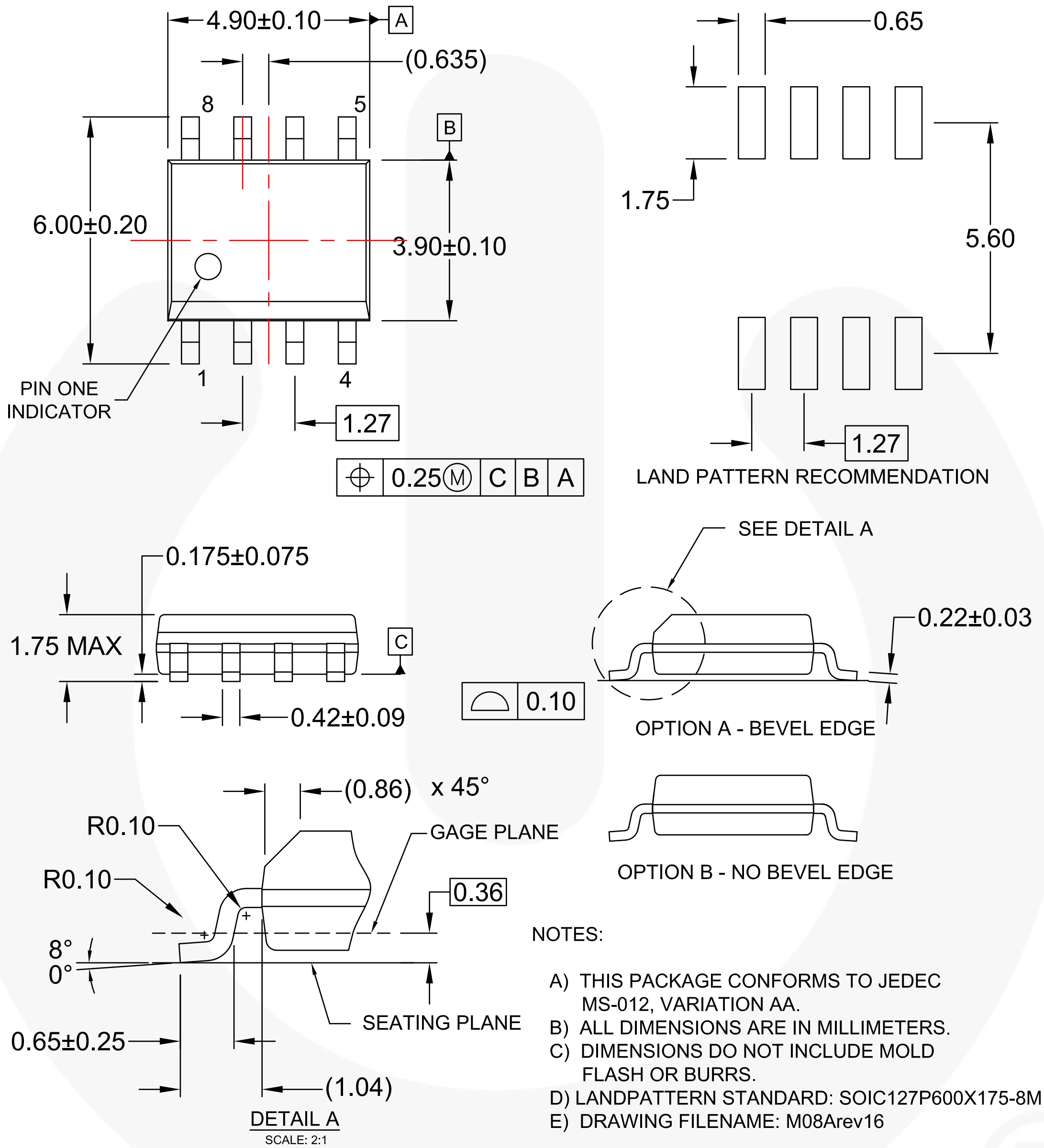


Figure 7. 5-LEAD, SC70, EIAJ SC-88A, 1.25MM WIDE

Physical Dimensions (Continued)

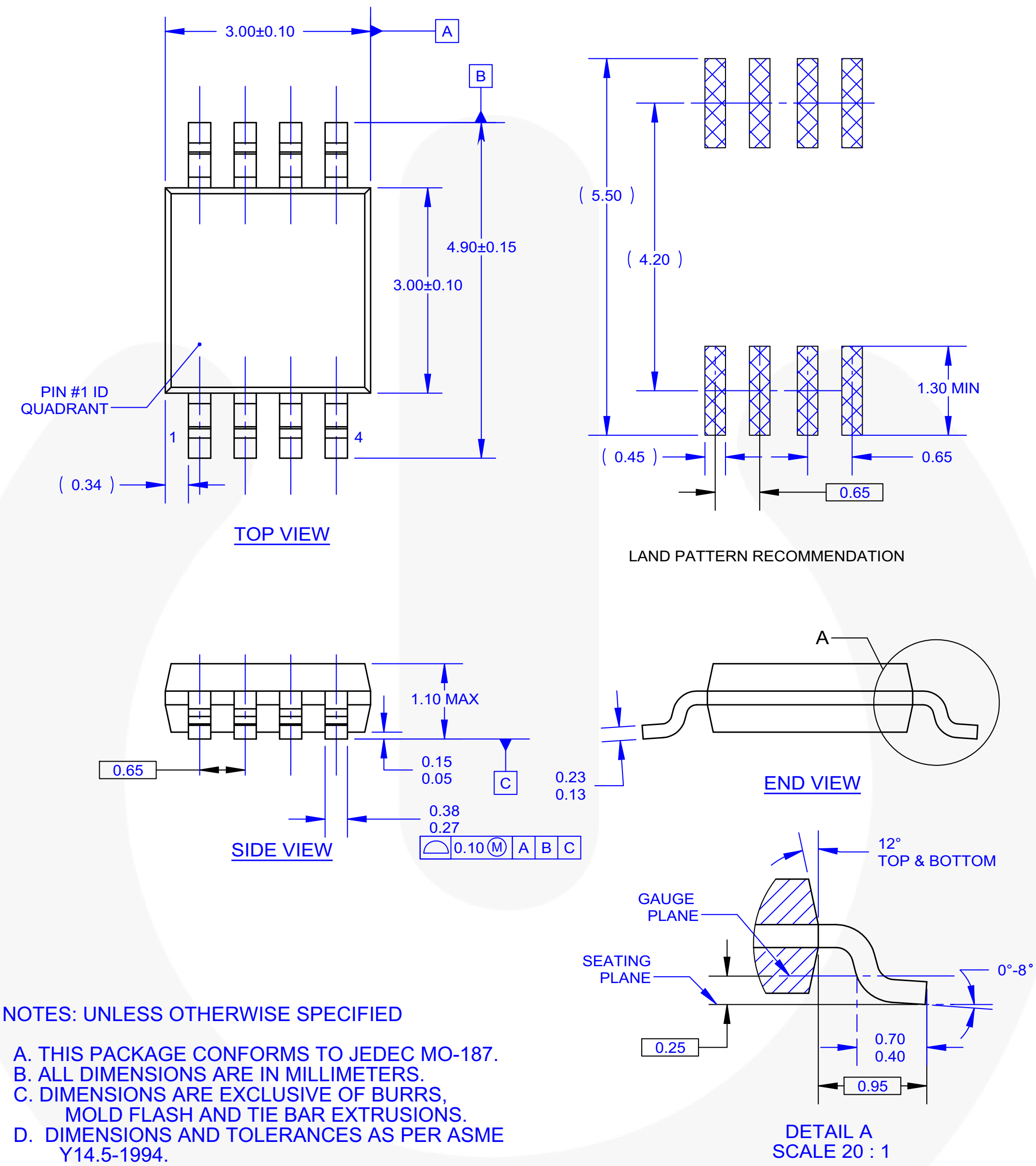


NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

Figure 8. 8-LEAD, SOIC, JEDEC MS-012, 0.150 INCH NARROW BODY

Physical Dimensions (Continued)

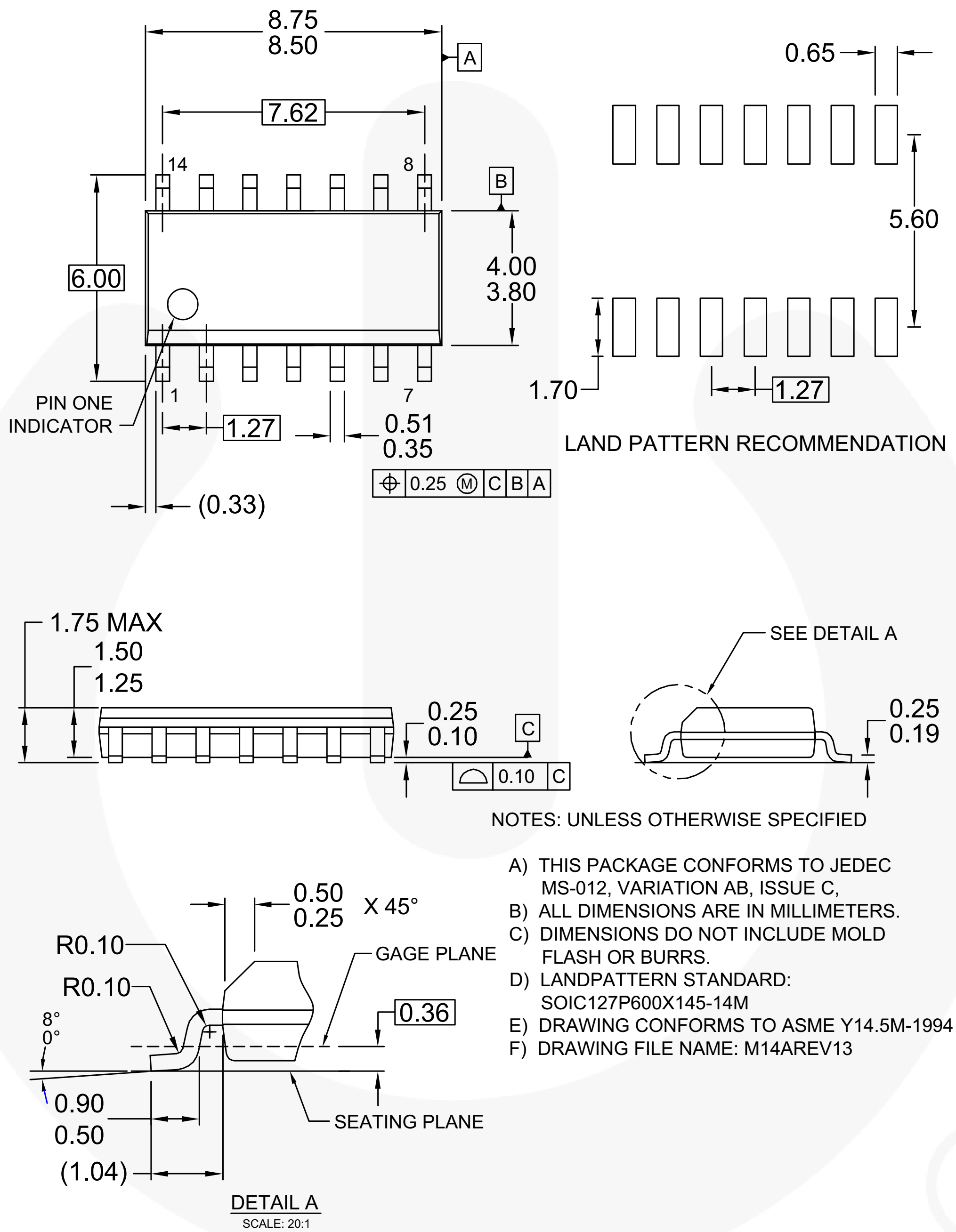


NOTES: UNLESS OTHERWISE SPECIFIED

A. THIS PACKAGE CONFORMS TO JEDEC MO-187.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES AS PER ASME Y14.5-1994.
E. LAND PATTERN AS PER IPC7351#TSOP65P490X110-8BL
F. FILE NAME: MKT-MUA08AREV4

Figure 9. 8-LEAD, MSOP, JEDEC MO-187, 3.0MM WIDE

Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X145-14M
E) DRAWING CONFORMS TO ASME Y14.5M-1994
F) DRAWING FILE NAME: M14AREV13

Figure 10. 14-LEAD, SOIC, JEDEC MS-012, 0.150 INCH NARROW BODY

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