

Display Elektronik GmbH

DATA SHEET

LCD MODULE

DEM 128128A SYH-PY

Product specification

CONTENTS

1. FUNCTIONS & FEATURES	2
2. BLOCK DIAGRAM	2
3. EXTERNAL DIMENSIONS	3
4. PIN ASSIGNMENT	3
5. PCB DRAWING	4
6. JUMPER SETTING.....	5
7. ABSOLUTE MAXIMUM RATINGS.....	5
8. ELECTRICAL CHARACTERISTICS.....	6
9. SED1335F TIMING DIAGRAMS.....	7
10. INSTRUCTION SET.....	9
11. DISPLAY CONTROL FUNCTIONS.....	29
12. CHARACTER GENERATOR.....	36
13. SYSTEM BUS INTERFACE.....	38
14. OSCILLATOR CIRCUIT.....	40
15. STATUS FLAG.....	40
16. RESET.....	42
17. APPLICATION NOTES	42
18. LCD MODULES HANDLING PRECAUTIONS.....	43
19. OTHERS	44

1. FUNCTIONS & FEATURES

- LCD-Type:

Version	LCD MODEL	LCD TYPE
DEM 128128A SYH-PY	STN	Transflective Positive Mode
DEM 128128A FYH-PY	FSTN	Transflective Positive Mode

- Viewing Direction : 6 O'clock
- Display contents : 128 x 128 Dots
- Driving Scheme : 1/128 Duty Cycle, 1/12 Bias, V(LCD)=17.5V
- Power Supply Voltage : 5.0V (typ.)
- Backlight Color : Yellow Green
- Backlight Type : LED (Side-Blacklight/Yellow-Green)
- Dot Size : 0.46(w) x 0.46(h) (mm)
- Dot Gap : 0.04 (mm)

2 . BLOCK DIAGRAM

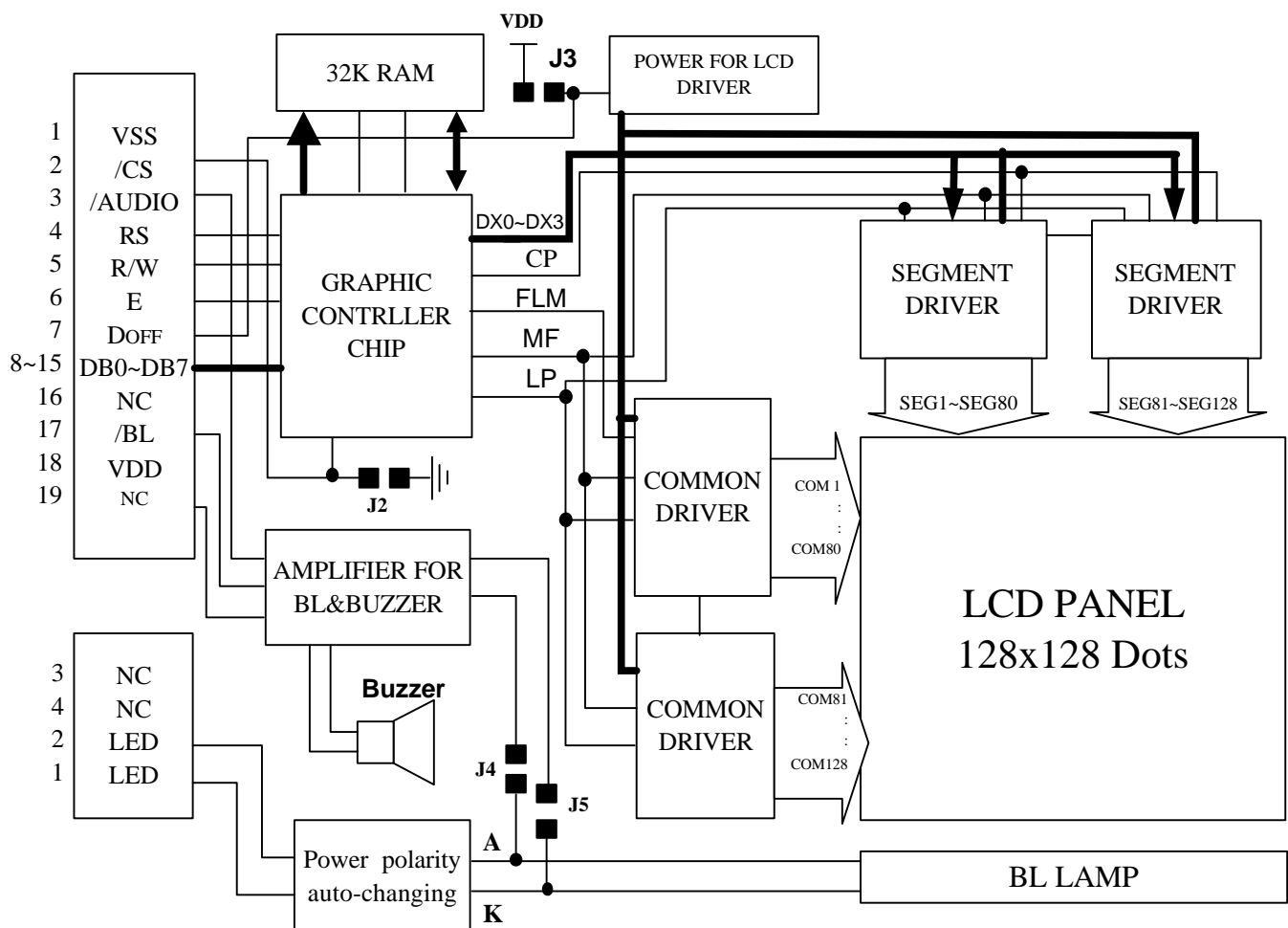


Figure 1.

3. External Dimensions

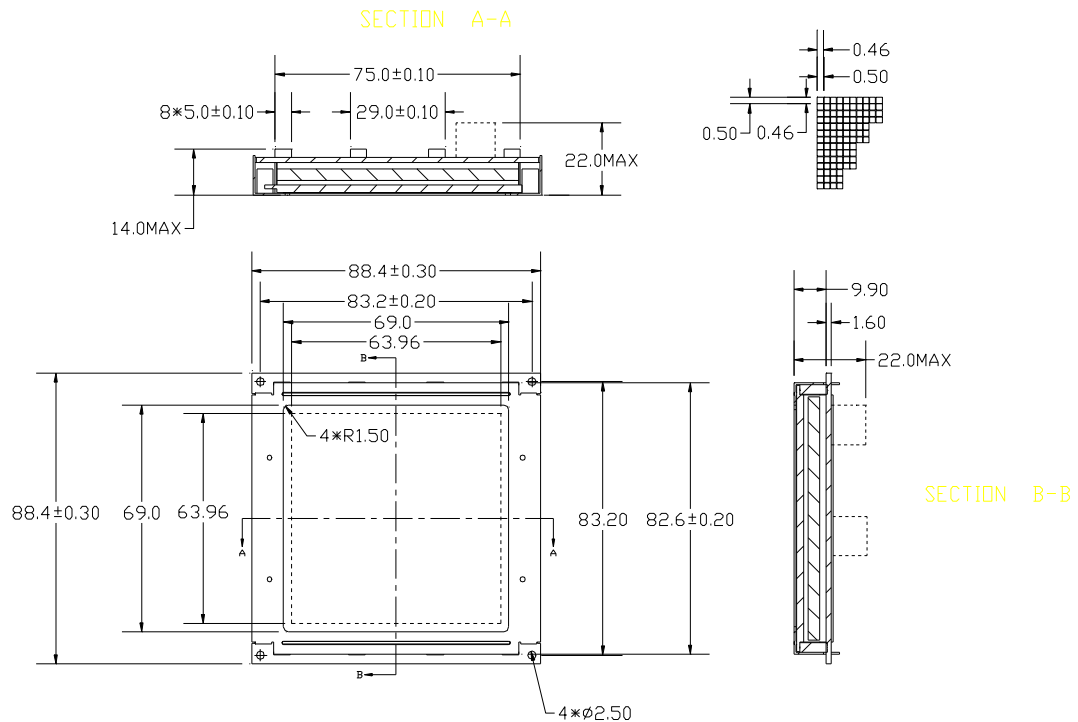


Figure 2.

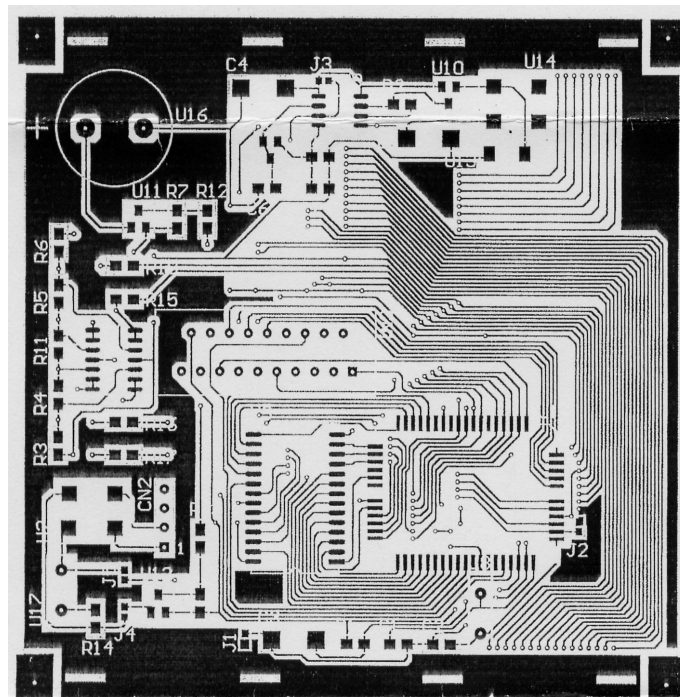
4. PIN Assignment

CONNECTOR "CN1"			
Pin No.	Symbol	LEVEL	Function
1	VSS	—	Terminal for ground .
2	/CS	—	Chip selection
3	/AUDIO	—	Audio control signal input (DC) . Audio=1 Buzzer ..OFF & Audio=0 BUZZER...ON
4	RS	H/L	Register select RS=1...Instruction RS=0...Data
5	R/W	H H -->> L	READ/WRITE R/W =1...Read R/W =0...Write
6	E	H H -->> L	Enable Singal E=H...Read E = H -->> L ... Write
7	DOFF	—	DOFF=1 VEE=ON & DOFF=0 VEE=OFF
8~15	DB0~DB7	H/L	8-bit data bus .
16	NC	—	No connection
17	/BL	—	Backlight control signal input BL=1...Backlight OFF BL=0...Backlight ON
18	VDD	+5V	Power supply terminal of module
19	NC	—	No connection
CONNECTOR "CN2"			
1	LED	—	Power for backlight (Any polarity)
2	LED	—	Power for backlight (Any polarity)
3	NC	—	No connection
4	NC	—	No connection

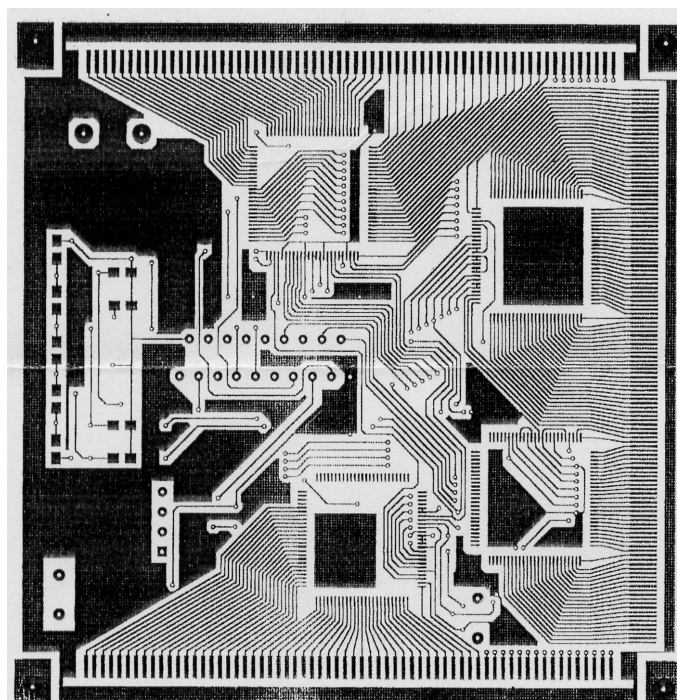
REMARK : LED Power ploarity auto-changing

5. PCB DRAWING

5.1 Top Layer



5.2 Bottom Layer



6. Jumper Setting

	SHORT	OPEN
J1	*The metal-bezel be on ground	_____
J2	/CS Control Disable	* /CS Control Enable
J3	DOFF Control Disable	* DOFF Control Enable
J4, J5	* /BL Control Enable	/BL Control Disable

REMARK: The asterisk is setting by the factory
The R14 is the LED resistor

7. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to 7.0	V
Input voltage range	V_{IN}	-0.3 to $V_{DD}+0.3$	V
Power dissipation	PD	300	mW
Operating temperature range	T_{opg}	-20 to 75	°C
Storage temperature range	T_{stg}	-20 to 75	°C
Soldering temperature(10 seconds).See note1.	T_{solder}	260	°C

Notes:

1. The humidity resistance of the flat package may be reduced if the package is immersed in solder.
Use a soldering technique that does not heatstress the package.
2. If the power supply has a high impedance, a large voltage differential can occur between the input and supply voltages. Take appropriate care with the power supply and the layout of the supply lines. (See section 6.2.)
3. All supply voltage are referenced to $V_{ss}=0V$.

8. Electrical Characteristics

VDD = 4.5 to 5.5V, VSS = 0V, Ta = -20 to 75°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V _{DD}		4,5	5.0	5,5	V
Register data retention voltage	V _{OH}		2.0	—	6.0	V
Input leakage current	I _{LI}	V _I =V _{DD} .See note 5.	—	0,05	2.0	μA
Output leakage current	I _{LO}	V _I =V _{SS} .See note5.	—	0.10	5.0	μA
Operating supply current	I _{opr}	See note 4.	—	11	15	Ma
Quiescent supply current	I _Q	Sleep mode, V _{osc1} =V _{/CS} =V _{/RD} =V _{DD}	—	0,05	20.0	μA
Oscillator frequency	f _{osc}	Measured at crystal, 47.5% duty cycle. See note 6.	1.0	—	10.0	MHZ
External clock frequency	f _{cl}		1.0	—	10.0	MHZ
Oscillator feedback resistance	R _f		0,5	1.0	3.0	Mohm
TTL						
HIGH-level input voltage	V _{IHT}	See note 1.	0.5V _{DD}	—	V _{DD}	V
LOW-level input voltage	V _{ILT}	See note 1.	V _{SS}	—	0.2V _{DD}	V
HIGH-level output voltage	V _{OHT}	I _{OH} =-5.0 mA.See note 1.	2,4	—	—	V
LOW-level output voltage	V _{OLT}	I _{OL} =5.0 mA.See note 1.	—	—	V _{SS} +0.4	V
CMOS						
HIGH-level input voltage	V _{IHC}	See note 2.	0.8V _{DD}	—	V _{DD}	V
LOW-level input voltage	V _{ILC}	See note 2.	V _{SS}	—	0.2V _{DD}	V
HIGH-level output voltage	V _{OHC}	I _{OH} =-2.0 mA.See note 2.	V _{DD} -0.4	—	—	V
LOW-level output voltage	V _{OLC}	I _{OH} =1.6 mA.See note 2.	—	—	V _{SS} +0.4	V
Open-drain						
LOW-level output voltage	V _{OLN}	I _{OL} =6.0 mA	—	—	V _{SS} +0.4	V
Schmitt-trigger						
Rising-edge threshold voltage	V _{T+}	See note 3.	0.5V _{DD}	0.7V _{DD}	0.8V _{DD}	V
Falling-edge threshold voltage	V _{T-}	See note 3.	0.2V _{DD}	0.3V _{DD}	0.5V _{DD}	V

Notes: D0 to D7,A0,/CS,/RD,/WR are TTL-level inputs.

9. SED1335F TIMING DIAGRAMS

9.1. 6800 family interface timing

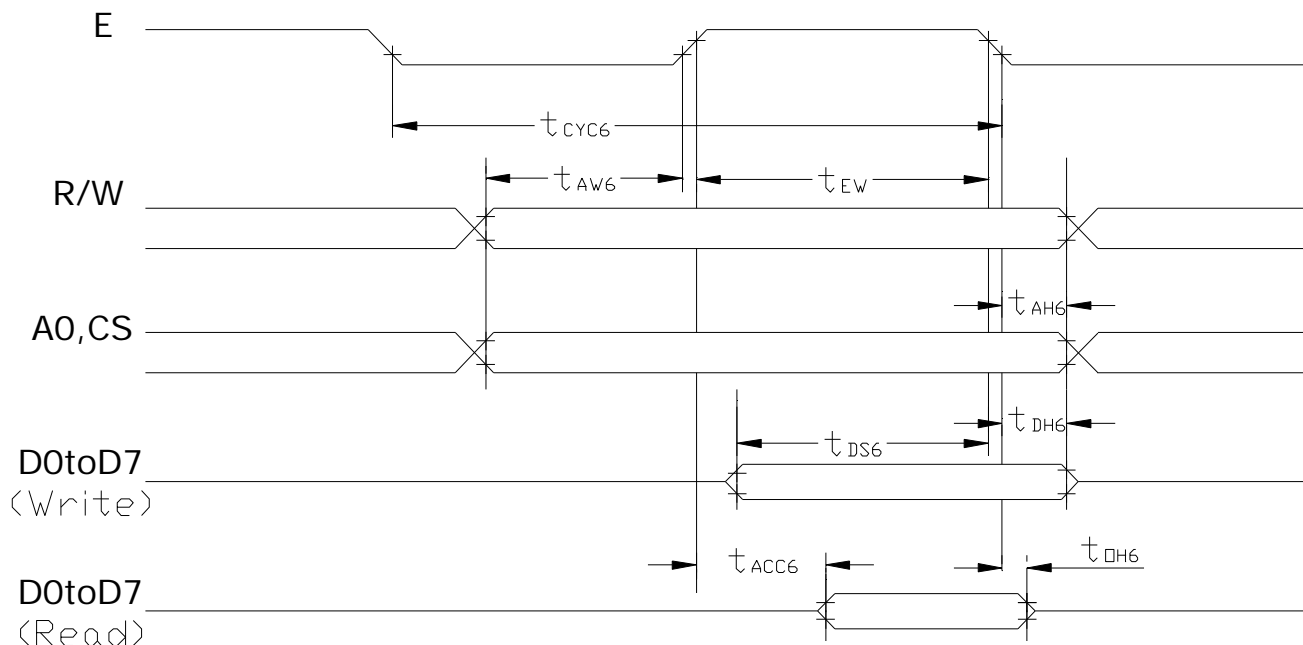


Figure 5.

Note : t_{CYC6} indicates the interval during which CS is LOW and E is HIGH .

$T_a = -20$ to 75°C

Signal	Symbol	Parameter	VDD=4.5 to 5.5V		VDD=2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{\text{CS}}$, R/W	t_{CYC6}	System cycle time	See note.	—	See note.	—	ns	CL=100 pF
	t_{AW6}	Address setup time	0	—	10	—	ns	
	t_{AH6}	Address hold time	0	—	0	—	ns	
D0 to D7	t_{DS6}	Data setup time	100	—	120	—	ns	
	t_{DH6}	Data hold time	0	—	0	—	ns	
	t_{OH6}	Output disable time	10	50	10	75	ns	
	t_{ACC6}	Access time	—	85	—	130	ns	
E	t_{EW}	Enable pulsewidth	120	—	150	—	ns	

Note: For memory control and system control commands:

$$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$$

For all other commands:

$$t_{CYC6} = 4t_C + t_{EW} + 30$$

9.2. SLEEP IN command timing

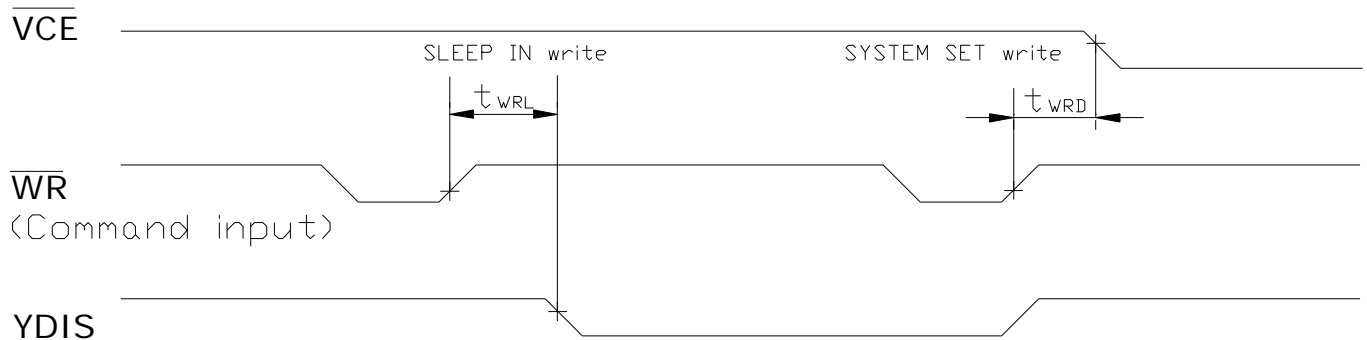


Figure 6.

 $T_a = -20 \text{ to } 75^\circ\text{C}$

Signal	Symbol	Parameter	VDD=4.5 to 5.5V		VDD=2.7 to 4.5V		Unit	Condition
			min	max	min	max		
\overline{WR}	t_{WRD}	\overline{VCE} falling-edge delay time	See note 1.	—	See note 1.	—	ns	CL=100
	t_{WRL}	\overline{YDIS} falling-edge delay time	—	See note 2.	—	See note 2.	ns	P _F

Notes:

1. $T_{WRD}=18t_C+t_{OSS}+40$ (T_{OSS} is the time delay from the sleep state until stable operation)
2. $T_{WRL}=36t_C*[TC/R]*[L/F]+70$

10. INSTRUCTION SET

10.1. The Command Set

Class	Command	Code												Hex	Command Description	command read	
		/RD	/WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	Parameters				
													No.of Bytes			Section	
System control	SYSTEM SET	1	0	1	0	1	0	0	0	0	0	0	40	Initialize device and display	8	8.2.1	
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53	Enter standby mode	0	8.2.2	
Display control	DISP ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58, 59	Enable and disable display and display flashing	1	8.3.1	
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Set display start address and display regions	10	8.3.2	
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Set cursor type	2	8.3.3	
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Set start address of character generator RAM	2	8.3.6	
	CSRDIR	1	0	1	0	1	0	0	1	1	CD	CD	4C to 4F	Set direction of cursor movement	0	8.3.4	
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Set horizontal scroll position	1	8.3.7	
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Set display overlay format	1	8.3.5	
Drawing control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Set cursor address	2	8.4.1	
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Read cursor address	2	8.4.2	
Memory control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Write to display memory	—	8.5.1	
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Read from display memory	—	8.5.2	

Notes:

- In general, the internal registers of the SED1335 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged.

2-byte parameter (where two bytes are treated as 1 data item) are handled as follows:

 - CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.
 - SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.
- APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

10.2. System Control Commands

10.2.1. SYSTEM SET

Initializes the device , sets the window sizes, and selects the LCD interface format . Since this command sets the basic operating parameters of the SED1335 series, an incorrect SYSTEM SET command may cause other commands to operate incorrectly .

MSB									LSB		
	D7	D6	D5	D4	D3	D2	D1	D0	A0	/WR	/RD
C	0	1	0	0	0	0	0	1	0	1	1
P1	0	0	IV	1	W/S	M2	M1	M0	0	0	1
P2	WF	0	0	0	0	← FX →			0	0	1
P3	0	0	0	0	← FY →			0	0	1	
P4	← C/R →							0	0	1	
P5	← TC/R →							0	0	1	
P6	← L/F →							0	0	1	
P7	← APL →							0	0	1	
P8	← APH →							0	0	1	

Figure 7. SYSTEM SET instruction

10.2.1.1 C

This control byte performs the following :

1. Resets the internal timing generator
2. Disables the display
3. Cancels sleep mode

Parameters following P1 are not needed if only canceling sleep mode .

10.2.1.2 M0

Selects the internal or external character generator ROM .The internal character generator ROM contains 160,5 x 7 pixel characters , as shown in figure 70. These characters are fixed at fabrication by the metallization mask . The external character generator ROM, on the other hand, can contain up to 256 user-defined characters . M0 = 0: Internal CG ROM M0 = 1: External CG ROM

Note that if the CG ROM address space overlaps the display memory address space, that portion of the display memory cannot be written to .

10.2.1.3 M1

Selects the memory configuration for user-definable characters. The CG RAM codes select one of the 64 codes shown in figure 46. M1 = 0 : No D6 correction .The CG RAM1 and CG RAM2 address spaces are not contiguous, the CG RAM1 address space is treated as character generator RAM, and the CG RAM2 address space is treated as character generator ROM . M1 = 1: D6 correction .

The CG RAM1 and CG RAM2 address spaces are contiguous and are both treated as character generator RAM .

10.2.1.4 . M

Selects the height of the character bitmaps. Characters more than 16 pixels high can be displayed by creating a bitmap for each portion of each character and using the SED1335 series graphics mode to reposition them.

M2 = 0: 8-pixel character height (2716 or equivalent ROM)

M2 = 1: 16-pixel character height (2732 or equivalent ROM)

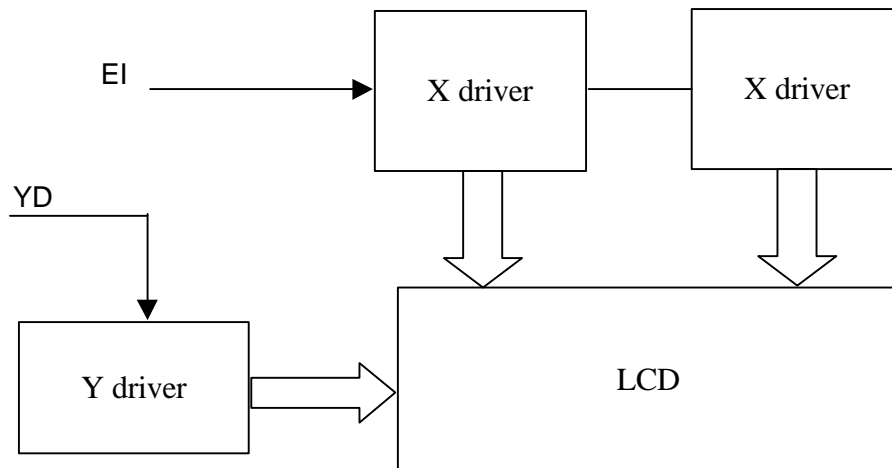


Figure 8.

10.2.1.5 . W/S

Selects the LCD drive method . W/S = 0: Single -panel drive W/S = 1 : Dual-panel drive

LCD parameters

Parameter	W/S = 0		W/S = 1	
	IV = 1	IV = 0	IV = 1	IV = 0
C/R	C/R	C/R	C/R	C/R
TC/R	TC/R	TC/R(See note 1.)	TC/R	TC/R
L/F	L/F	L/F	L/F	L/F
SL1	00H to L/F	00H to L/F +1 (See note 2.)	(L/F)/2	(L/F)/2
SL2	00H to L/F	00H to L/F +1 (See note 2.)	(L/F)/2	(L/F)/2
SAD1	First screen block	First screen block	First screen block	First screen block
SAD2	Second screen block	Second screen block	Second screen block	Second screen block
SAD3	Third screen block	Third screen block	Third screen block	Third screen block
SAD4	Invalid	Invalid	Fourth screen block	Fourth screen block
Cursor movement range	Continuous movement over whole screen		Above-and-below configuration: continuous movement over whole screen	

Notes :

1. See table 26 for further details on setting the C/R and TC/R parameters when using the HDOT SCR Command .
2. The value of SL when IV = 0 is equal to the value of SL when IV = 1 , plus one .

10.2.1.6. IV

Screen origin compensation for inverse display . IV is usually set to 1.

The best way of displaying inverted characters is to Exclusive-OR the text layer with the graphics background layer . However, inverted characters at the top or left of the screen are difficult to read as the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these characters .

The IV flag causes the SED1335 series to offset the text screen against the graphics back layer by one vertical pixel . Use the horizontal pixel scroll function (HDOT SCR) to shift the text screen 1 to 7 pixels to the right . All characters will then have the necessary surrounding background pixels that ensure easy reading of the inverted characters .

See Section 10.5 for information on scrolling .

IV = 0 : Screen top-line correction V = 1 : No screen top-line correction

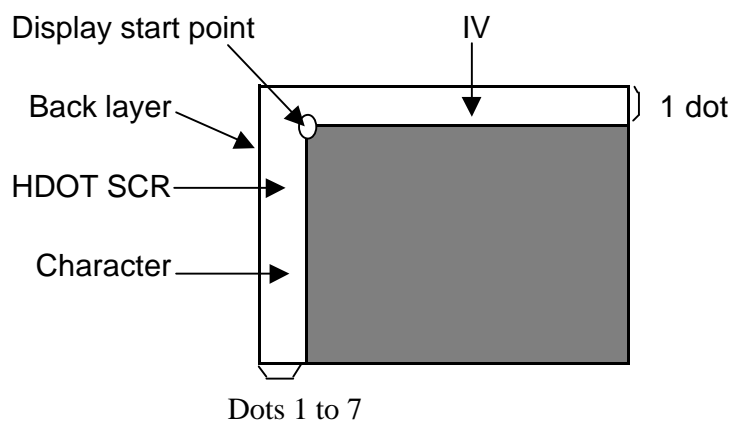


Figure 9. IV and HDOT SCR adjustment

10.2.1.7. FX

Define the horizontal character size . The character width in pixels is equal to $FX + 1$, where FX can range from 00 to 07H inclusive . If data bit 3 is set (FX is in the range 08 to 0FH) and an 8-pixel font is used, a space is inserted between characters .

Horizontal character size selection

FX					[FX] character width (pixels)
HEX	D3	D2	D1	D0	
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8

Since the SED1335 series handles display data in 8-bit units, characters larger than 8 pixels wide must be formed from 8-pixel segments. As Figure 6 shows, the remainder of the second eight bits are not displayed . This also applies to the second screen layer .

In graphics mode, the normal character field is also eight pixels . If a wider character field is used, any remainder in the second eight bits is not displayed .

(CONTINUED)

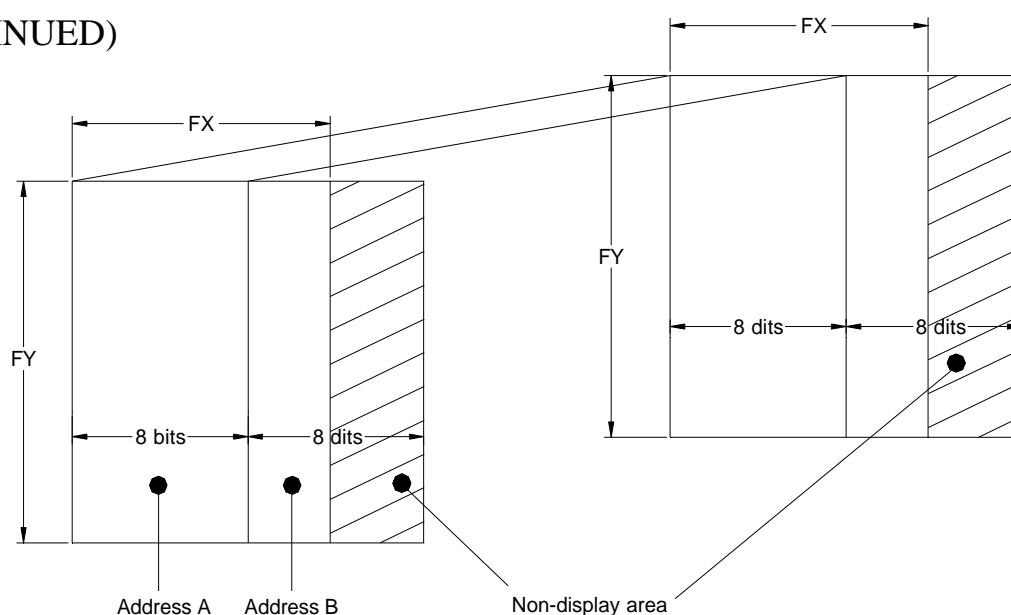


Figure 10.

10.2.1.8. WF

Selects the AC frame waveform period. WF is usually set to 1.

WF = 0 : 16-line AC drive WF = 1 : two - frame AC drive

In two-frame AC drive , the WF period is twice the frame period . In 16-line AC drive .WF inverts every 16 lines .Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles .

10.2.1.9. FV

Sets the vertical character size, The height in pixels is equal to FY + 1 .

FY can range from 00 to 0FH inclusive . Set FY to zero (vertical size equals one) when in graphics mode.

Vertical character size selection

FY					[FY] character height
HEX	D3	D2	D1	D0	(pixels)
00	0	0	0	0	1
01	0	0	0	1	2
↓	↓	↓	↓	↓	↓
07	0	1	1	1	8
↓	↓	↓	↓	↓	↓
0E	1	1	1	0	15
0F	1	1	1	1	16

10.2.1.10. C/R

Sets the address range covered by one display line, that is , the number of characters less one , multiplied by the number of horizontal bytes per character.

C/R can range from 0 to 239.

For example. If the character width is 10 pixels, then the address range is equal to twice the number of characters, less 2. See Section 16.1.1 for the calculation of C/R .

[C/R] cannot be set to a value greater than the address range. It can, however, be set smaller than the address range, in which case the excess display area is blank. The number of excess pixels must not exceed 64 .

10.2.1.10. C/R

Display line address range

C/R									C/R] bytes per display lin
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	0	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
4F	0	1	0	0	1	1	1	1	80
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
EE	1	1	1	0	1	1	1	0	239
FF	1	1	1	0	1	1	1	1	240

10.2.1.11. TC/R

Sets the length, including horizontal blanking, of one line. The line length is equal to TC/R + 1, where TC/R can range from 0 to 255

TC/R must be greater than or equal to C/R + 4. Provided this condition is satisfied, [TC/R] can be set according to the equation given in section 16.1.1 in order to hold the frame period constant and minimize jitter for any given main oscillator frequency, fosc.

Line length selection

TC/R									[TC/R] Line length (bytes)
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
52	0	1	0	1	0	0	1	0	83
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

10.2.1.12. L/F

Sets the height, in lines, of a frame. The height in lines is equal to L/F + 1, where L/F can range from 0 to 255.

Frame height selection

L/F									[L/F] Lines per frame
HEX	D7	D6	D5	D4	D3	D2	D1	D0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	0	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

If W/S is set to 1, selecting two-screen display, the number of lines must be even and L/F must, therefore, be an odd number.

10.2.1.13. AP

Defines the horizontal address range of the virtual screen. APL is the least significant byte of the address .

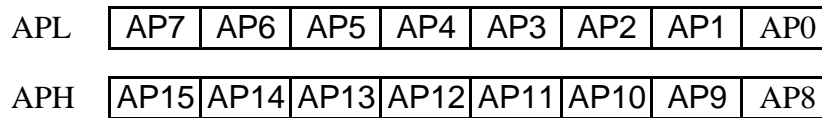
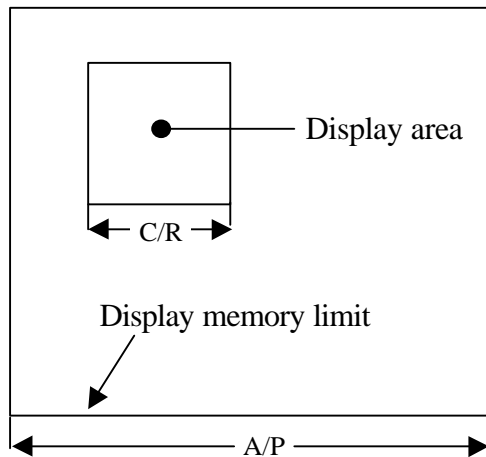


Figure 11. AP parameters



Hex code				[AP] address
APH		APL		per line
0	0	0	0	0
0	0	0	1	1
↓	↓	↓	↓	↓
0	0	5	0	80
↓	↓	↓	↓	↓
F	F	F	F	$2^{16} - 2$
F	F	F	F	$2^{16} - 1$

Figure 12. AP and C/R relationship

10.2.2. SLEEP IN

Places the system in standby mode. This command has no parameter bytes. At least one blank frame after receiving this command, the SED1335F halts all internal operations, including the oscillator, and enters the sleep state. Blank data is sent to the X-drivers, and Y-drivers have their bias supplies turned off by the YDIS signal. Using the YDIS signal to disable the Y-drivers guards against any spurious displays.

The internal registers of the SED1335 series maintain their values during the sleep state. The display memory control pins maintain their logic levels to ensure that the display memory is not corrupted .

The SED1335 series can be removed from the sleep state by sending the SYSTEM SET command with only the P1 parameter. The DISP ON command should be sent next to enable the display .

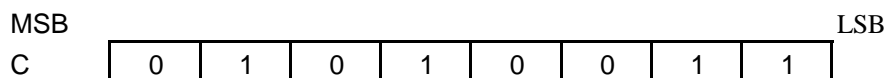


Figure SLEEP IN instruction

1. The YDIS signal goes LOW between one and two frames after the SLEEP IN command is received. Since YDIS forces all display driver outputs to go to the deselected output voltage, YDIS can be used as a power-down signal for the LCD unit. This can be done by having YDIS turn off the relatively high-power LCD driver supplies at the same time as it blanks the display .
2. Since all internal clocks in the SED1335 series are halted while in the sleep state, a DC voltage will be applied to the LCD panel if the LCD drive supplies remain on .
3. Note that, although the bus lines become high impedance in the sleep state, pull-up or resistors on the bus will force these lines to a known state .

10.3. Display Control Commands

10.3.1. Display ON/OFF

Turns the whole display on or off. The single-byte parameter enables and disables the cursor and layered screens, and sets the cursor and screen flash rates. The cursor can be set to flash over one character or over a whole line .

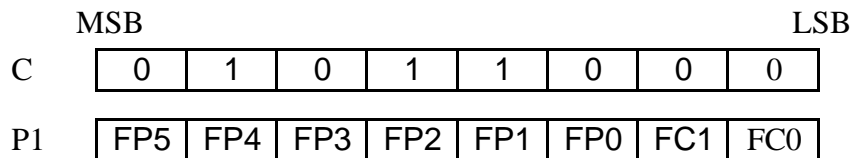


Figure 13. DISP ON/OFF parameters

10.3.1.1. D

Turns the display ON or OFF. The D bit takes precedence over the FP bits in the parameter .

D = 0 : Display OFF

D = 1 : Display ON

10.3.1.2. FC

Enables/disables the cursor and sets the flash rate. The cursor flashes with a 70% duty cycle (ON/OFF) .

Cursor flash rate selection

FC1	FC0	Cursor display	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at $f_{FR}/32$ Hz (approx. 2 Hz)
1	1		Flash at $f_{FR}/64$ Hz (approx. 1 Hz)

Note :

As the MWRITE command always enables the cursor, the cursor position can be checked even when performing consecutive writes to display memory while the cursor is flashing .

10.3.1.3. FP

Each pair of bits in FP sets the attributes of one screen block, as follows .

The display attributes are as follows :

Screen block attribute selection

FP1	FP0	First screen block (SAD1)	
FP3	FP2	Second screen block (SAD2, SAD4). See note .	
FP5	FP4	Third screen block (SAD3)	
0	0	OFF (blank)	
0	1	ON	No flashing
1	0		Flash at $f_{FR}/32$ Hz (approx. 2 Hz)
1	1		Flash at $f_{FR}/4$ Hz (approx. 16 Hz)

Note :

If SAD4 is enabled by setting W/S to 1, FP3 and FP2 control both SAD2 and SAD4. The attributes of SAD2 and SAD4 cannot be set independently .

10.3.2. SCROLL

10.3.2.1. C

Sets the scroll start address and the number of lines per scroll block .Parameters P₁ to P₁₀ can be omitted if not required. The parameters must be entered sequentially as shown in Figure 14.

	MSB				LSB				
C	0	1	0	0	0	1	0	0	
P1	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 1L)
P2	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 1H)
P3	L7	L6	L5	L4	L3	L2	L1	L0	(SL 1)
P4	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 2L)
P5	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 2H)
P6	L7	L6	L5	L4	L3	L2	L1	L0	(SL 2)
P7	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 3L)
P8	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 3H)
P9	A7	A6	A5	A4	A3	A2	A1	A0	(SAD 4L)
P10	A15	A14	A13	A12	A11	A10	A9	A8	(SAD 4H)

Figure 14. SCROLL instruction parameters

Note : Set parameters P9 and P10 only if both two-screen drive (W/S = 1) and two-layer configuration are selected. SAD4 is the fourth screen block display start address .

Screen block start address selection

SL1, SL2									[SL] screen lines
HEX	L7	L6	L5	L4	L3	L2	L1	L0	
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	0	2
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
7F	1	1	1	1	1	1	1	1	128
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

10.3.2.2. SL1, SCL2

SL1 and SL2 set the number of lines per scrolling screen, The number of lines is SL1 or SL2 plus one. The relationship between SAD, SL and the display mode is describe below.

Text display mode

Text display mode			
W/S	Screen	First Layer	Second Layer
0	First screen block	SAD1	SAD2
	Second screen block	SL1	SL2
	Third screen block (partitioned screen)	SAD3 (See note 1) Set both SL1 and SL2 to L/F + 1 If not using a partitioned screen .	
	Screen configuration example :		

W/S	Screen	First Layer	Second Layer
1	Upper screen block	SAD1 SL1	SAD2 SL2
	Lower screen	SAD3 (See note 2.)	SAD4 (See note 2.)
	Set both SL1 and SL2 to $((L/F) / 2 + 1)$.		
	Screen configuration example : 		

Notes :

1. SAD3 has the same value as either SAD1 or SAD2 , whichever has the least number of lines (set by SL1 and SL2).
2. Since the parameters corresponding to SL3 and SL4 are fixed by L/F,they do not have to be set in this mode.

(CONTINUED)

Graphics Display Mode

Graphics display mode				
W/S	Screen	First Layer	Second Layer	Third Layer
0	Two - layer composition	SAD1 SL1	SAD2 SL2	
	Upper screen	SAD3 (See note 3) Set both SL1 and SL2 to L/F + 1 if not using a partitioned screen .		
	Screen configuration example :			
W/S	Three-layer configuration	SAD1 SL1 = L/F + 1	SAD2 SL2 = L/F + 1	SAD3 —
1	Screen configuration example :			

(CONTINUED)

Graphics Display Mode

W/S	Screen	First Layer	Second Layer	Third Layer
1	Upper-screen	SAD1 SL1	SAD2 SL2	—
	Lower screen	SAD3 (See note 2.)	SAD4 (See note 2.)	—
	Set both SL1 and SL2 to $((L/F) / 2 + 1)$.			
	Screen configuration example :			

Note :

- 1.SAD3 has the same value as either SAD1 or SAD2 , whichever has the least number of lines (set by SL1 and SL2) .
- 2.Since the parameters corresponding to SL3 and SL4 are fixed by L/F , they dot not have to be set .
- 3.If, and only if , $W/S = 1$, the differences between SL1 and $(L/F + 1) / 2$, and between SL2 and $(L/F + 1) / 2$, are blanked .

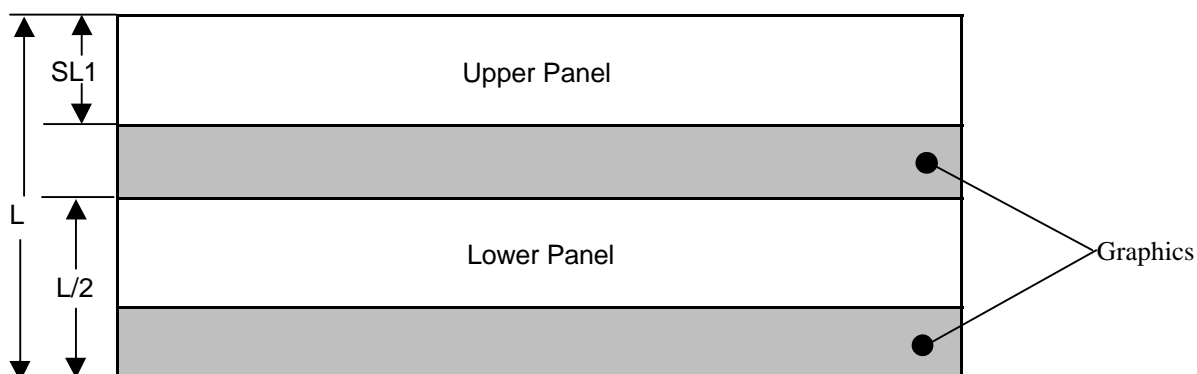


Figure 15. Two-panel display height

10.3.3. CSRFORM

Sets the cursor size and shape. Although the cursor is normally only used in text displays, it may also be used in graphics displays when displaying special characters.

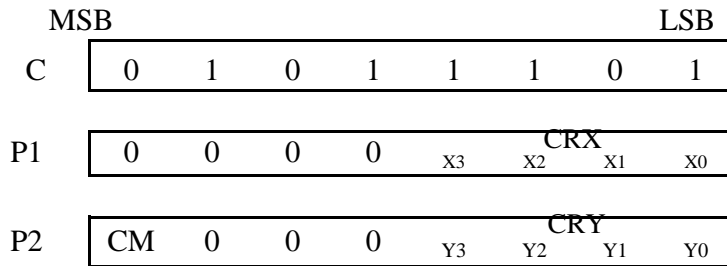


Figure 16. CSRFORM parameter bytes

10.3.3.1. CRX

Sets the horizontal size of the cursor from the character origin. CRX is equal to the cursor size less one. CRX must be less than or equal to FX.

Table 14. Horizontal cursor size selection

CRX					[CRX] cursor width (pixels)
HEX	X3	X2	X1	X0	
0	0	0	0	0	Legal
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
4	0	1	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

10.3.3.2. CRY

Sets the location of an underscored cursor in lines, from the character origin. When using a block cursor, CRY sets the vertical size of the cursor from the character origin. CRY is equal to the number of lines less one.

Table 15. Cursor height selection

CRX					[CRX] cursor height (lines)
HEX	X3	X2	X1	X0	
0	0	0	0	0	1
1	0	0	0	1	2
↓	↓	↓	↓	↓	↓
8	1	0	0	0	9
↓	↓	↓	↓	↓	↓
E	1	1	1	0	15
F	1	1	1	1	16

(CONTINUED)

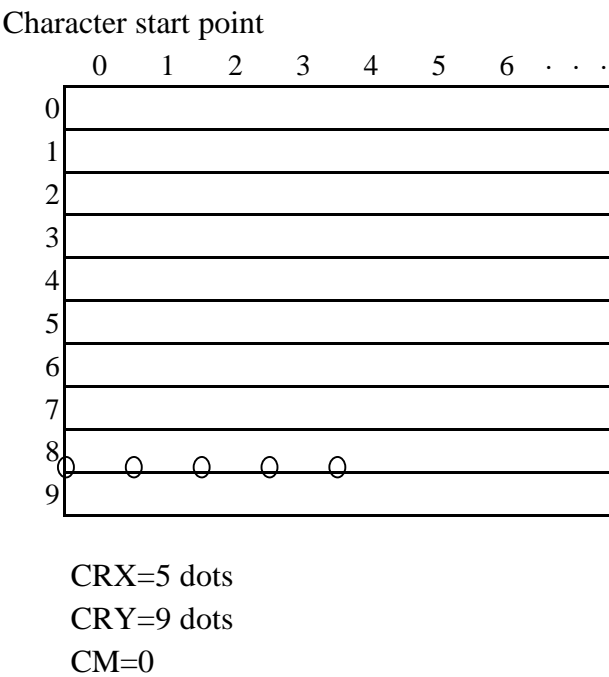


Figure 17. Cursor size and position

10.3.3.3. CM

Sets the cursor shape. Always set CM to 1 when in graphics mode.

CM=0: Underscore cursor

CM=1:Block cursor

10.3.4. CSRDIR

Sets the direction of automatic cursor increment. The cursor can move left right one character, or up or down by the number of bytes specified by the address pitch, AP. When reading from and writing to display memory, this automatic cursor increment controls the display memory address increment on each read or write.

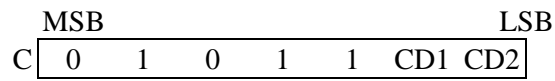


Figure 18. CSRDIR parameters

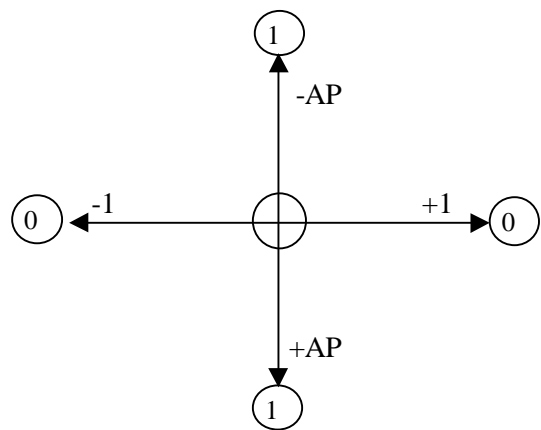


Figure 19. Cursor direction

Table 16. Cursor shift direction

C	CD1	CD0	Shift direction
4CH	0	0	Right
4DH	0	1	Left
4EH	1	0	Up
4FH	1	1	Down

10.3.5. OVLATY

Selects layered screen composition and screen text/graphics mode.

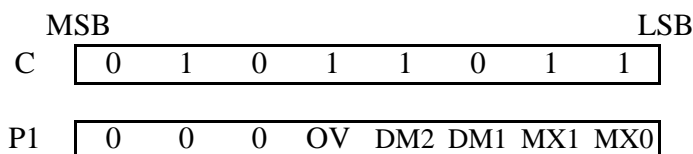


Figure 20. OVLAY parameters

10.3.5.1. MX0,MX1

MX0 and MX1 set the layered screen composition method, which can be either OR, AND, Exclusive-OR or Priority-OR. Since the screen blocks, when using a layer divided into two screen blocks, different composition methods cannot be specified for the individual screen blocks.

The Priority-OR mode is the same as the OR mode unless flashing of individual screens is used.

Table 17. Composition method selection

MX1	MX0	Function	Composition Method	Applications
0	0	L1 U L2 U L3	OR	Underlining, rules, mixed text and graphics
0	1	$(L1 \oplus L2) U L3$	Exclusive-OR	Inverted characters, flashing regions underlining
1	0	$(L1 \cap L2) U L3$	AND	Simple animation, three-dimensional appearance
1	1	$L1 > L2 > L3$	Priority-OR	

Notes:

L1: First layer (text or graphics). If text is selected, layer L3 cannot be used.

L2: Second layer (graphics only)

L3: Third layer (graphics only)

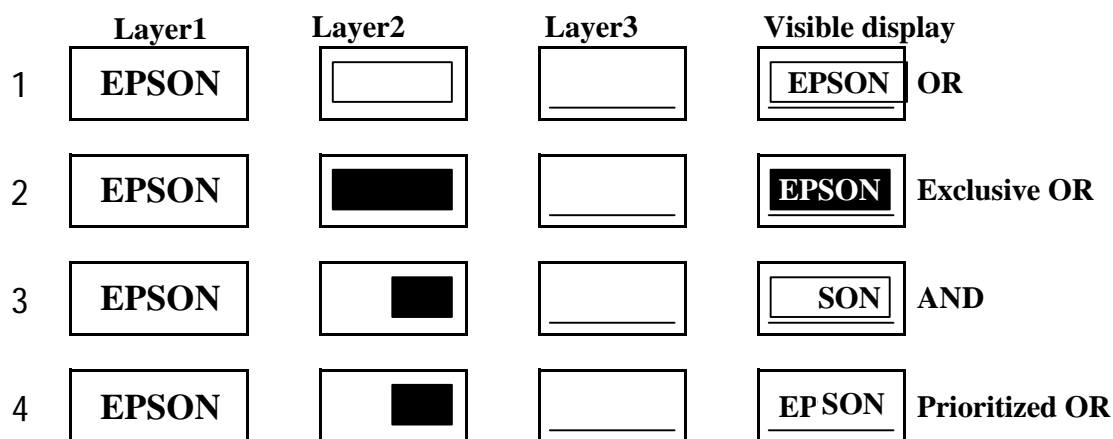


Figure 21. Combined layer display

Notes:

L1: Not flashing

L2: Flashing at 1 HZ

L3: Flashing at 2 HZ

10.3.5.2. DM1,DM2

DM1 and DM2 specify the display mode of screen blocks 1 and 3, respectively.

DM1/2=0: Text mode

DM1/2=0: Graphics mode

Note1: Screen blocks 2 and 4 can only display graphics.

Note2: DM1 and DM2 must be the same, regardless of the setting of W/S.

10.3.5.3. OV

Specifies two-or three-layer composition in graphics mode.

OV=0: Two-layer composition

OV=1: Three-layer composition .

Set OV to 0 for mixed text and graphics mode.

10.3.6. CGRAM ADR

Specifies the CG RAM start address.

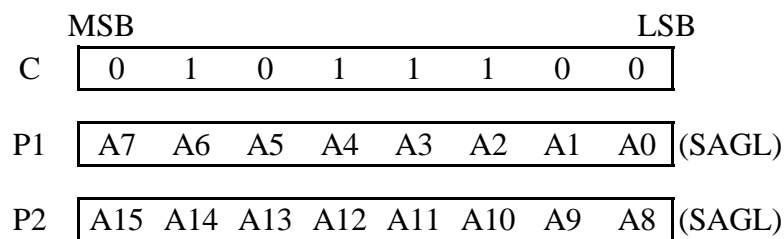


Figure 22. CGRAM ADR parameters

Note

See section 10 for information on the SAG parameters.

10.3.7. HDOT SCR

While the SCROLL command only allows scrolling by characters, HDOT SCR allows the screen to be scrolled horizontally by pixels. HDOT SCR cannot be used on individual layers.

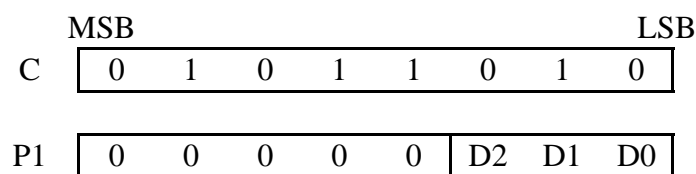


Figure 23. HDOT SCR parameters

10.3.7.1. D0 to D2

Specifies the number of pixels to scroll. The C/R parameter has to be set to one more than the number of horizontal characters before using HDOT SCR. Smooth scrolling can be simulated if the controlling microprocessor repeatedly issues the HDOT SCR command to the SED 1335 series. See Section 9.5 for more information on scrolling the display.

10.4. Drawing Control Commands

10.4.1. CSRW

The 16-bit cursor address register contains the display memory address of the data at the cursor position as shown in Figure 24.

Note that the microprocessor cannot directly access the display memory.

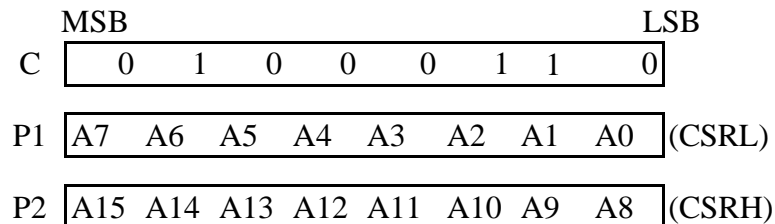
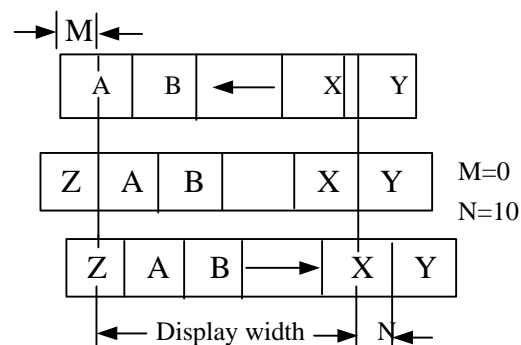


Figure 24. CSRW parameters

Table 18 . Scroll step selection(continued)

P1				Number of pixels to scroll
HEX	D2	D1	D0	
00	0	0	0	0
01	0	0	1	1
02	0	1	0	2
↓	↓	↓	↓	↓
06	1	1	0	6
07	1	1	1	7



M/N is the number of bits(dots) that parameter 1(p1) is incremented/decremented by.

Figure 25. Horizontal scrolling

The MREAD and MWRITE commands use the address in this register.

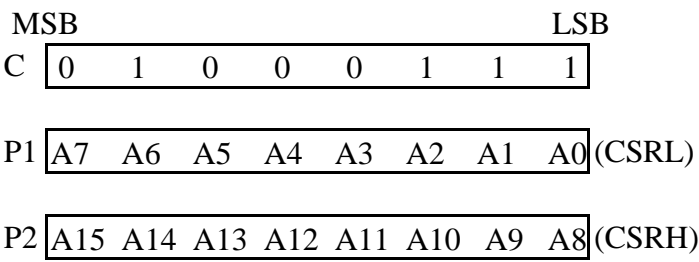
The cursor address register can only be modified by the CSRW command, and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling.

10.4.2. CSRR

Reads from the cursor address register. After issuing the command, the data read address is read twice, for the low byte and then high byte of the register.

If a new address is not set, display memory accesses will be from the last set address or the address after previous automatic increments.

If a new address is not set, display memory accesses will be from the last set address or the address after previous automatic increments.



10.5. Memory Control Commands

10.5.1. MWRITE

The microprocessor may write a sequence of data bytes to display memory by issuing the MREAD command and then writing the bytes to the SED 1335 series. There is no need for further MWRITE commands or for the microprocessor to update the cursor address register after each byte as the cursor address is automatically incremented by the amount set with CSRDIR, in preparation for the next data write.

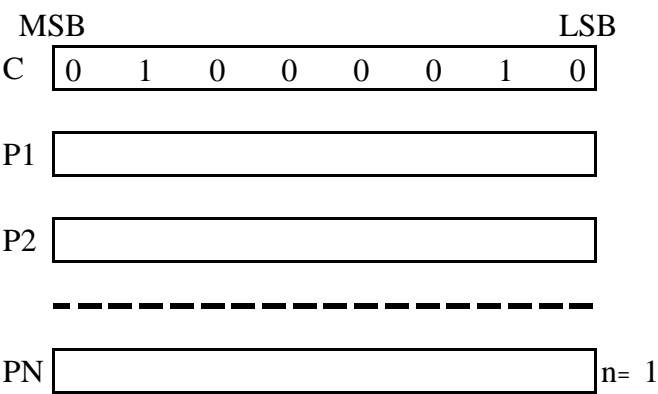


Figure 26. MWRITE parameters

Note:
P1, P2,...,Pn: display data.

10.5.2. MREAD

Puts the SED 1335 series into the data output state.Each time the microprocessor reads the buffer, the cursor address is incremented by the amount set by CSRDIR and the next data byte fetched from memory, so a sequence of data bytes may be read without further MREAD commands or by updating the cursor address register.

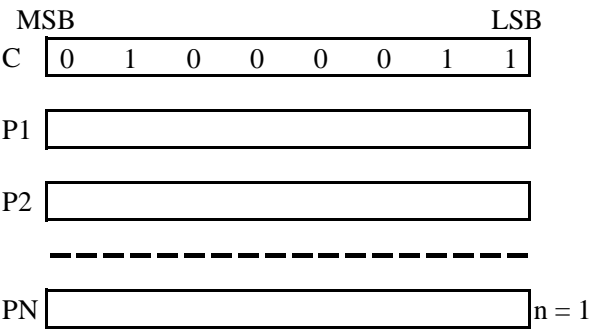


Figure 27. MREAD parameters

11. DISPLAY CONTROL FUNCTIONS

11.1. Character Configuration

Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.

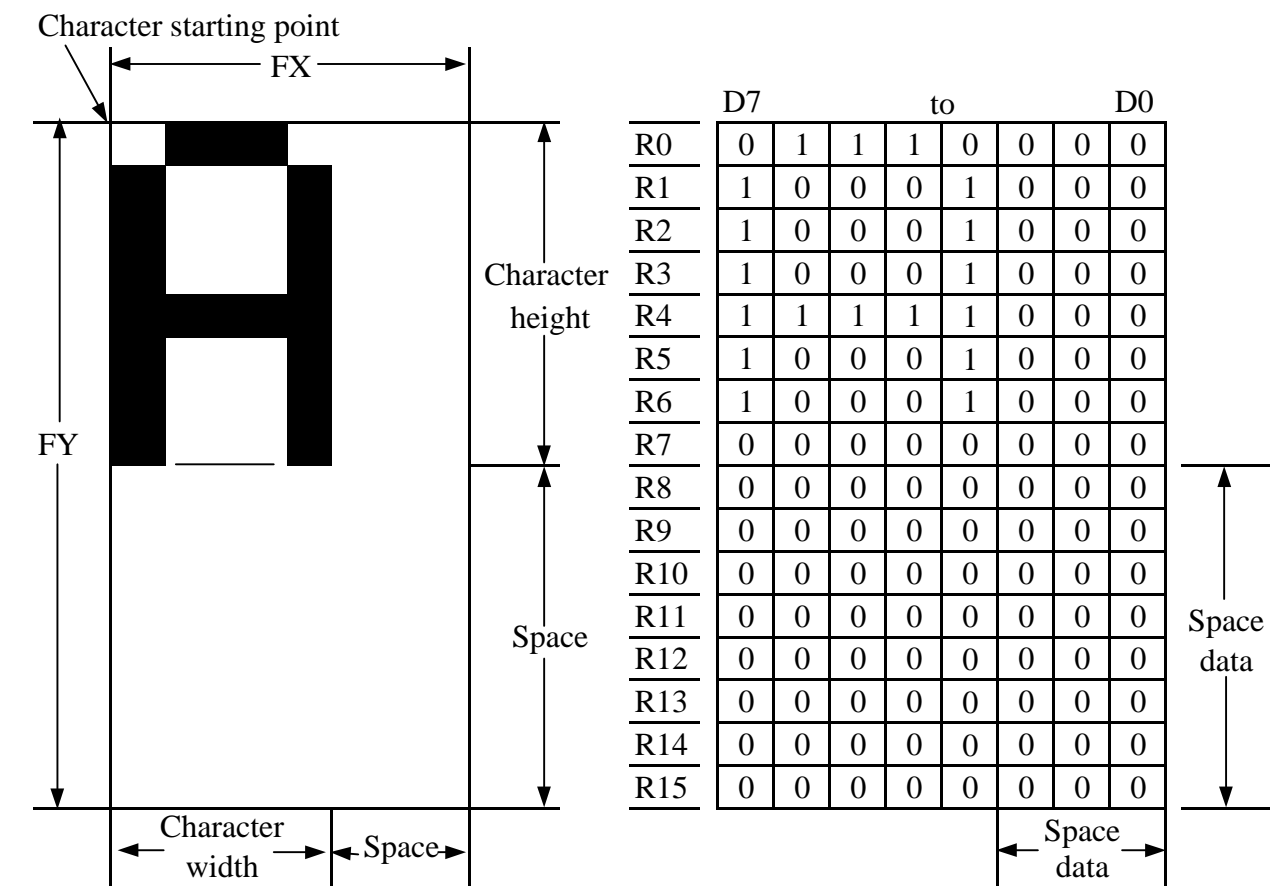


Figure 28. Example of character display ([FX]= 8) and generator bitmap

If the area outside the character bitmap contains only zeros, the displayed character size can easily be increased by increasing FX and FY, as the zeros ensure that the extra space between displayed characters is blank. The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.

(CONTINUED)

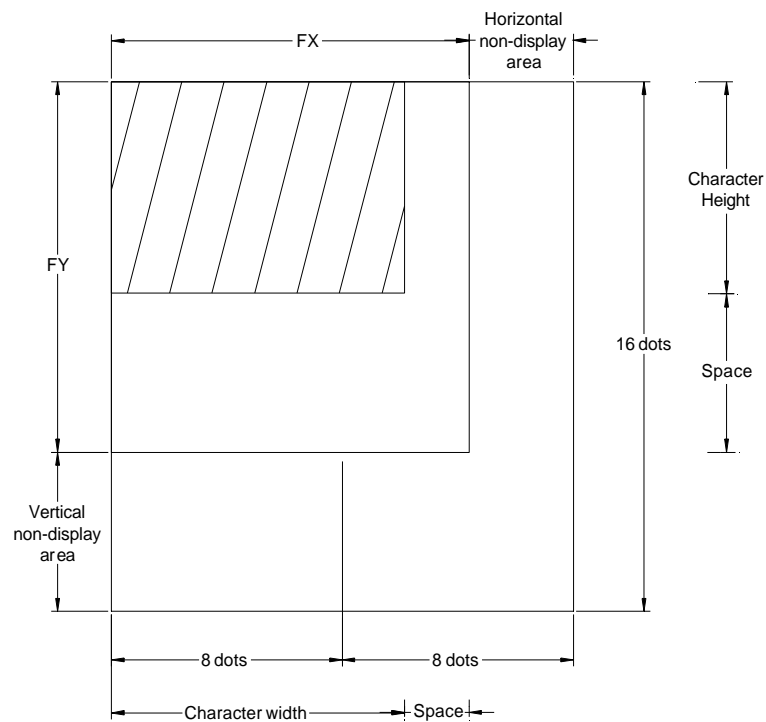


Figure 29. Character width greater than one byte wide ([FX] = 9)

Note : The SED1335 series does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row., even though the character image requires only one .

(CONTINUED)

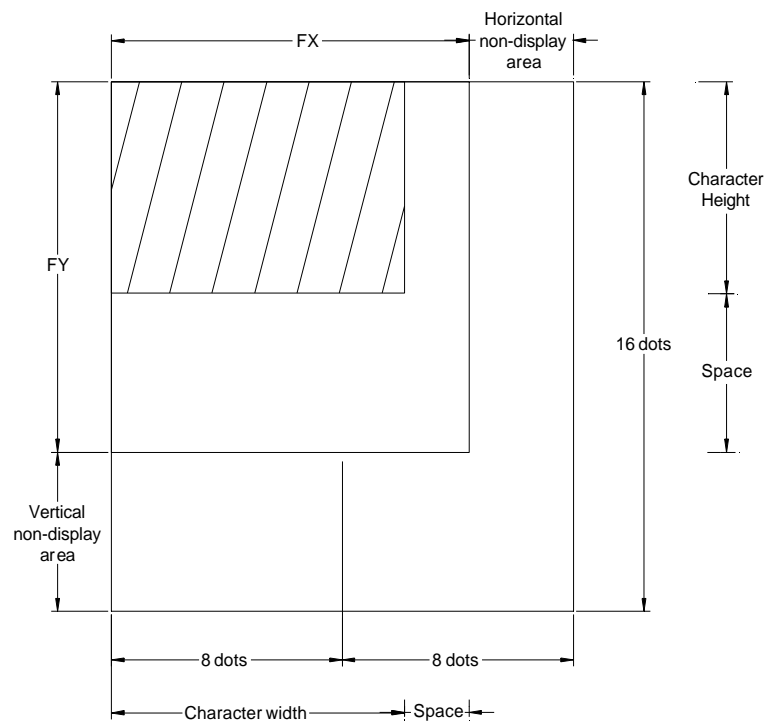


Figure 29. Character width greater than one byte wide ([FX] = 9)

Note : The SED1335 series does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row., even though the character image requires only one .

11.2. Cursor Control

11.2.1. Cursor register function

The SED 1335 series cursor address register functions as both the displayed cursor position address register. and the display memory access address register. When accessing display memory outside the actual screen memory, the address register must be saved before accessing the memory and restored after memory access is complete.

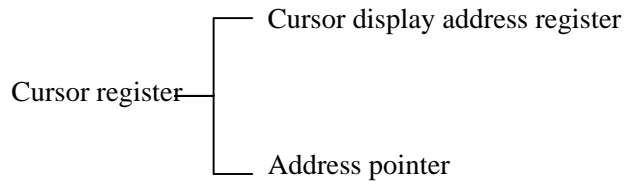


Figure 30. Cursor addressing

Note that the cursor may disappear from the display if the cursor address remains outside the displayed screen memory for more than a few hundred milliseconds.

11.2.2. Cursor movement

On each memory access, the cursor address register changes by the amount previously specified with CSRDIR, automatically moving the cursor to the desired location.

11.2.3. Cursor display layers

Although the SED 1335 series can display up to three layers, the cursor is displayed in only one of these layers:

Two-layer configuration: First layer (L1)

Three-layer configuration: Third layer (L3)

The cursor will not be displayed if it is moved outside the memory for its layer. Layers may be swapped or the cursor layer moved within the display memory if it is necessary to display the cursor on a layer other than the present cursor layer.

Although the cursor is normally displayed for character data, the SED 1335 series may also display a dummy cursor for graphical characters. This is only possible if the graphics screen is displayed, the text screen is turned off and the microprocessor generates the cursor control address.

(CONTINUED)

D=1

FC1=0

FC0=1

Cursor ON

FP1=0

FP0=0

Block screen 1(character screen) OFF

FP3=0

FP2=1

Block screen 2(graphics screen) ON

Consider the example of displaying Chinese characters on a graphics screen. To write the display data, the cursor address is set to the second screen block, but the cursor is not display .

To display the cursor, the cursor address is set to an address within the blank text screen block. Since the automatic cursor increment is in address units, not character units, the controlling microprocessor must set the cursor address register when moving the cursor over the graphical characters.

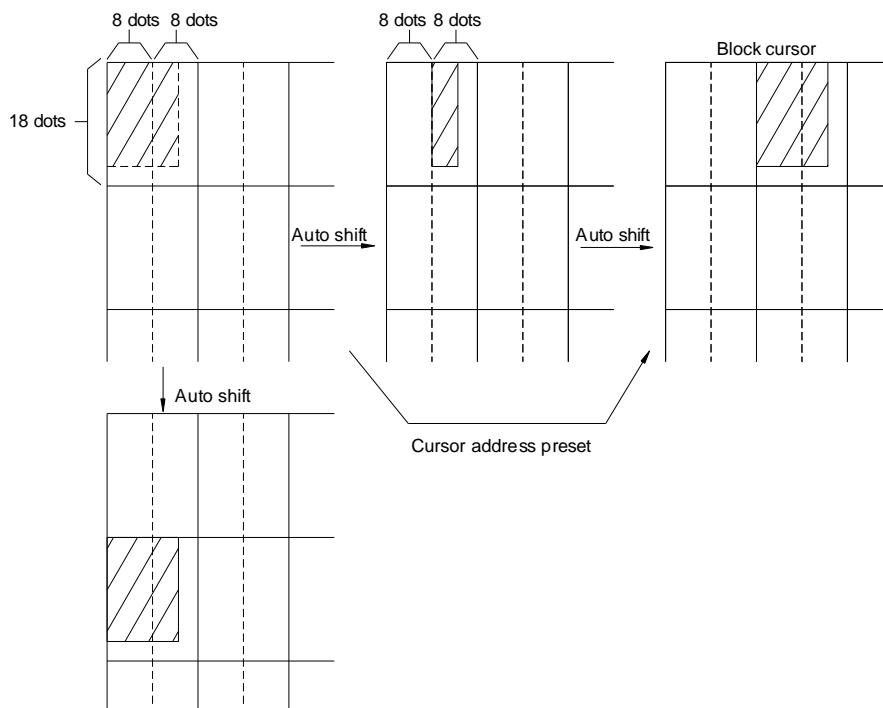


Figure 31. Cursor movement

If no text screen is displayed, only a bar cursor can be displayed at the cursor address.

If the first layer is a mixed text and graphics screen and the cursor shape is set to a block cursor, the SED1335 series automatically decides which cursor shape to display. On the text screen it displays a block cursor, and on the graphics screen, a bar cursor .

11.3. Scrolling

The controlling microprocessor can set the SED 1335 series scrolling modes by overwriting the scroll address registers SAD1 to SAD4, and by directly setting the scrolling mode and scrolling rate.

11.3.1. On-page scrolling

The normal method of scrolling within a page is to move the whole display up one line and erase the bottom line.

Since the SED 1335 series does not automatically erase the bottom line, it must be erased with blanking data when changing the scroll address register.

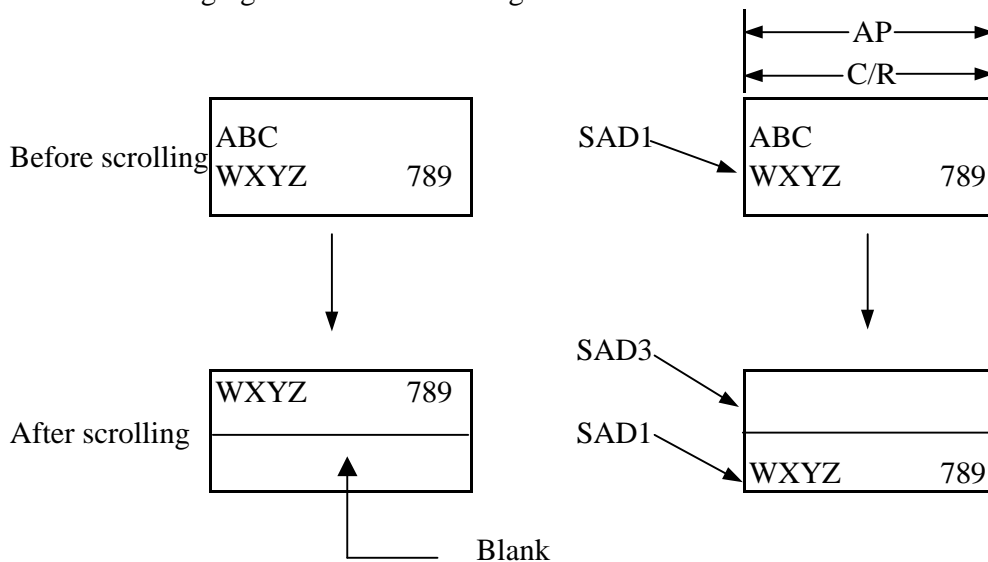


Figure 32. On-page scrolling

11.3.2. Inter-page scrolling

Scrolling between pages and page switching can be performed only if the display memory capacity is greater than one screen.

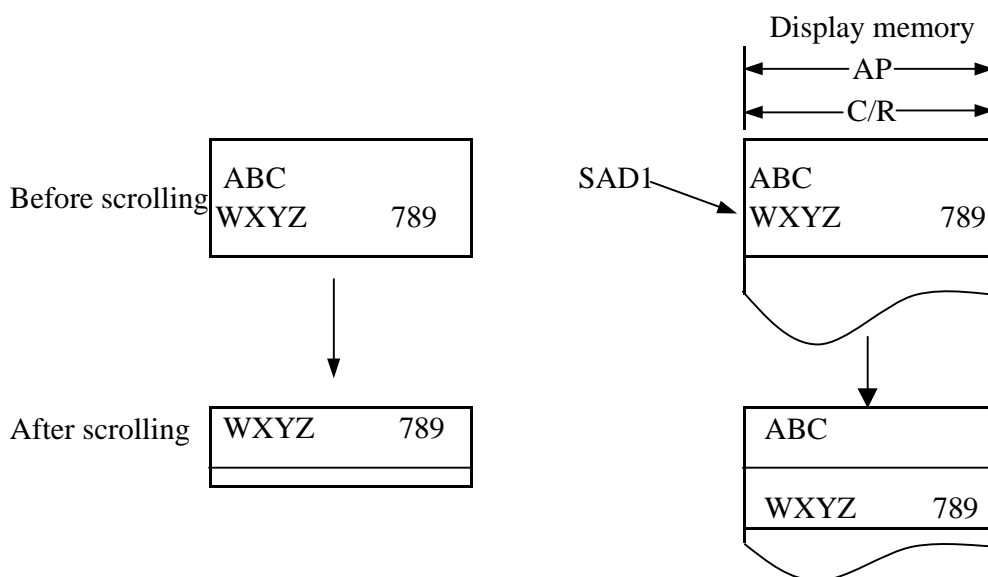


Figure 33. Inter-page scrolling

11.3.3. Horizontal scrolling

The display can be scrolled horizontally in one-character units, regardless of the display memory capacity.

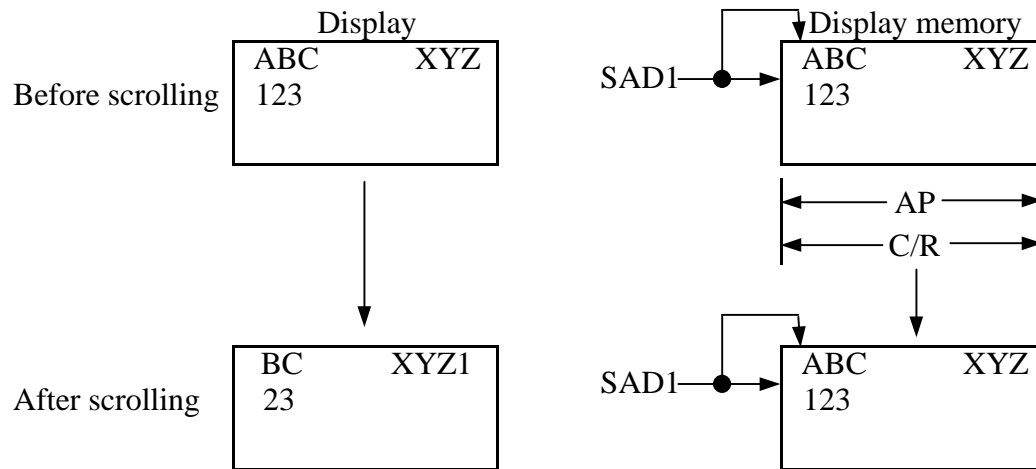


Figure 34. Horizontal wraparound scrolling

11.3.4. Bidirectional scrolling

Bidirectional scrolling can be performed only if the display memory is larger than the physical screen both horizontally and vertically. Although scrolling is normally done in single-character units, the HDOT SCR command can be used to scroll horizontally in pixel units. Single-pixel scrolling both horizontally and vertically can be performed by using the SCROLL and HDOT SCR commands. See Section 16.4

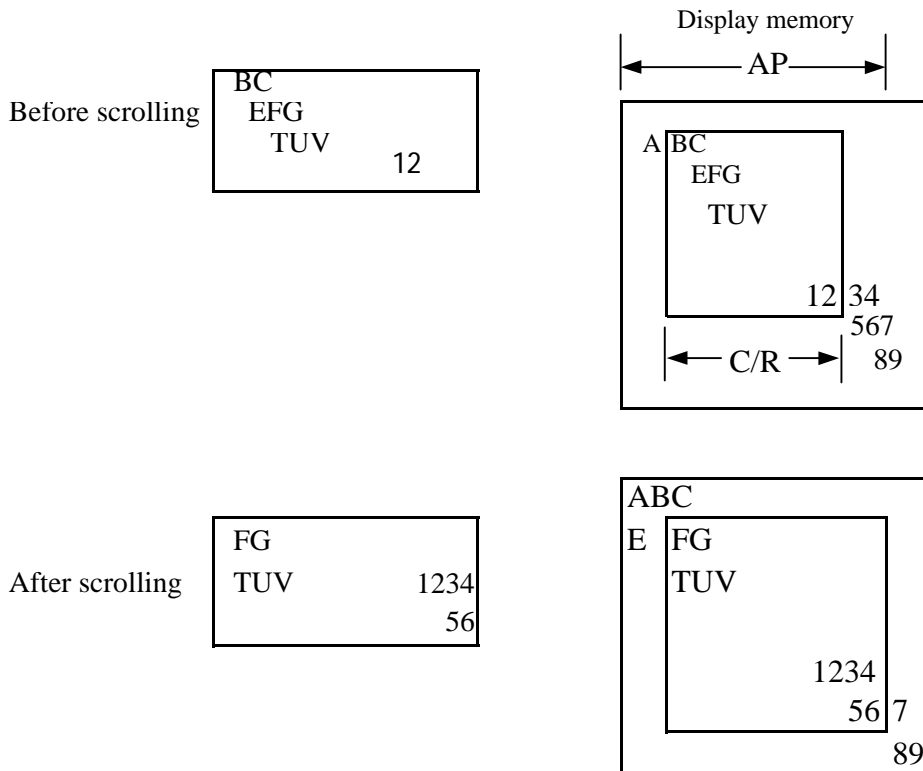


Figure 35. Bidirectional scrolling

13.3.5. Scroll units

Tale 19. Scroll units

Mode	Vertical	Horizontal
Text	Characters	Pixels or characters
Graphics	Pixels	Pixels

Note that in a divided screen, each block cannot be independently scrolled horizontally in pixel units.

12. CHARACTER GENERATOR

12.1. CG Characteristics

12.1.1. Internal character generator

The internal character generator is recommended for minimum system configurations containing a SED 1335 series, display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator use a CMOS mask ROM, it is also recommended for low-power applications.

- 5*7-pixel font (See Section 17.)
- 160 JIS standard characters
- Can be mixed with character generator RAM (maximum of 64 CG RAM characters)
- Can be automatically spaced out up to 8*16 pixels

12.1.2. External character generator ROM

The external CG ROM can be used when fonts other than those in the internal ROM are needed. Data is stored in the external ROM in the same format used in the internal ROM. (See Section 10.3.)

- Up to 8*8-pixel characters (M2=0) or 8*16-pixel characters (M2=1)
- Up to 256 characters (192 if used together with the internal ROM)
- Mapped into the display memory address space at F000H to F7FFH (M2=0) or F000H to FFFFH (M2=1).
- Characters can be up to 8*16-pixels; however, excess bits must be set to zero.

12.1.3. Character generator RAM

The user can freely use the character generator RAM for storing graphics characters. The character generator RAM can be mapped by the microprocessor anywhere in display memory, allowing effective use of unused address space.

- Up to 8*8-pixel characters (M2=0) or 8*16 character (M2=1)
- Up to 256 character if mapped at F000H to FFFFH (64 if used together with character generator ROM)
- Can be mapped anywhere in display memory address space if used with the character generator ROM
- Mapped into the display memory address space at F0000H to F7FFFH if not used with the character generator ROM (more than 64 characters are in the CGRAM). Set SAG0 to F000H and M1 to zero when defining characters number 193 upwards.

12.2. Setting the Character Generator Address

The CG RAM addresses in the VRAM address space are not mapped directly from the address in the SAG register. The data to be displayed is at a CG RAM address calculated from SAG + ROW select address. This mapping is shown in Table 21 and 22.

Table 21. Character fonts, number of lines = 8 (M2=0, M1=0)

SAG		A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code		0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ROW select address		0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CG RAM address		VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Table 22. Character fonts, 9=number of lines =16 (M2=1, M1=0)

SAG		A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code		0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ROW select address		0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CG RAM address		VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

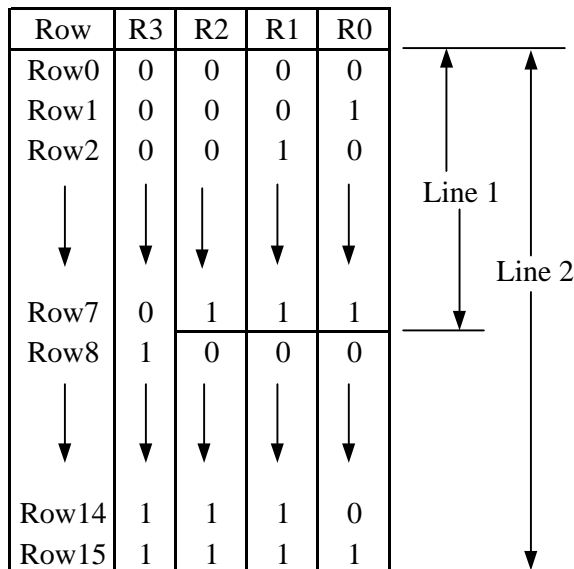


Figure 36. Row select address

Note: Lines=1: lines in the character bitmap=8

Lines=2: lines in the character bitmap=9

12.2.1. M1=1

The SED 1335 series automatically converts all bits set in bit 6 of character code for CG RAM 2 to zero. Because of this, the CG RAM data areas become contiguous in display memory.

When writing data to CG RAM:

Calculate the address as for M1=0.

Change bit 6 of the character code from “1” to “0”.

12.3. Character codes

The following figure shows the character codes and the codes allocated to CG RAM. ALL codes can be used by the CG RAM if not using the internal ROM.

Upper 4 bits																
Lower 4 bits	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0				0	@	P	'	p								
1			!	1	A	Q	a	q								
2			"	2	B	R	b	r								
3			#	3	C	S	c	s								
4			\$	5	D	T	d	t								
5			%	5	E	U	e	u								
6			&	6	F	V	f	v								
7			'	7	G	W	g	w								
8			(8	H	X	h	x								
9)	9	I	Y	i	y								
A			*	:	J	Z	j	z								
B			+V	;	K	[k	{								
C			,	<	L	?	l	!								
D			.	=	M]	m	}								
E			..	>	N	^	n	>								
F			/	?	O	_	o	>								

Figure 37. On- chip character codes

13. System Bus Interface

SEL1,SEL2,A0,/RD,/WR and /CS are used as control signals for the microprocessor data bus.A₀ is normally connected to the lowest bit of the system address bus . SEL1 and SEL2 change the operation of the /RD and /WR pins to enable interfacing to either an 8080 or 6800 family bus, and should have a pull-up or pull-down resistor, With microprocessors using an 8080 family interface, the SED1335 series is normally mapped into the I/O address space.

13.1.1 8080 Series

8080 series interface signals

A0	/RD	/WR	Function
0	0	1	Status flag read
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

13.1.2 6800 Series

6800 series interface signals

A0	/RD	E	Function
0	1	1	Status flag read
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

13.2. Microprocessor Synchronization

The SED1335 series interface operates at full bus speed, completing the execution of each command within the cycle time, TCYC. The controlling microprocessor's performance is thus not hampered by polling or handshaking when accessing the SED1335 series.

Display flicker may occur if there is more than one consecutive access that cannot be ignored within a frame. The microprocessor can minimize this either by performing these accesses intermittently, or by continuously checking the status flag (D6) and waiting for it to become HIGH.

13.2.1. Display status indication output

When \overline{CS} , A0 and \overline{RD} are LOW, D6 functions as the display status indication output. It is HIGH during the TV-mode vertical retrace period or the LCD-mode horizontal retrace period, and LOW during the period the controller is writing to the display. By monitoring D6 and writing to the data memory only during retrace periods, the display can be updated without causing screen flicker.

13.2.2. Internal register access

The SYSTEM SET and SLEEP IN commands can be used to perform input/output to the SED1335 series independently of the system clock frequency. These are the only commands that can be used while the SED1335 series is in sleep mode.

13.2.3. Display memory access

The SED1335 series supports a form of pipelined processing, in which the microprocessor synchronizes its processing to the SED1335 series timing. When writing, the microprocessor first issues the MWRITE command. It then repeatedly writes display data to the SED1335 series using the system bus timing. This ensures that the microprocessor is not slowed down even if the display memory access times are slower than the system bus access times. See Figure 38.

When reading, the microprocessor first issues the MREAD command, which causes the SED1335 series using the system bus timing. With each read, the SED1335 series reads the next data item from the display memory ready for the next read access. See Figure 39.

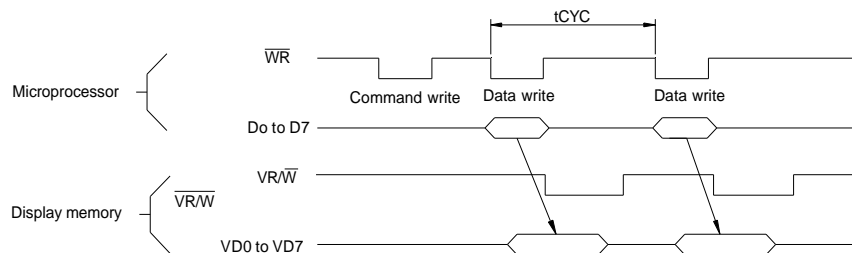


Figure 38. Display memory write cycle

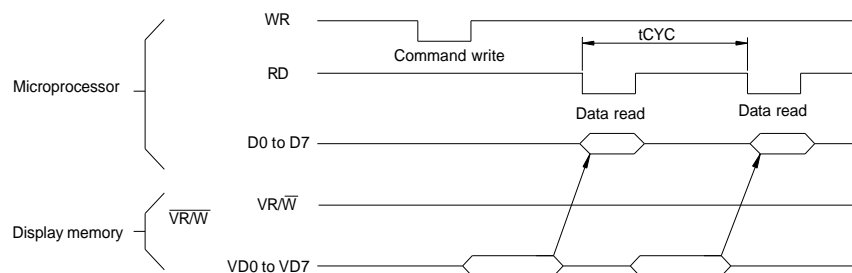


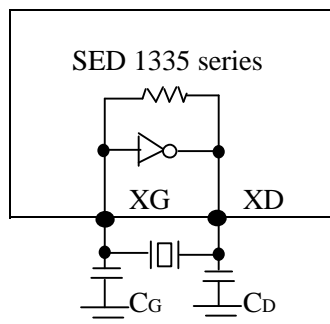
Figure 39 Display memory read cycle

Note: A possible problem with the display memory read cycle is that the system bus access time, t_{ACC} , does not depend on the display memory access time, t_{ACV} . The microprocessor may only make repeated reads if the read loop time exceeds the SED1335 series cycle time, t_{CYC} . If it does not, NOP instructions may be inserted in the program loop. t_{ACC} , t_{ACV} and t_{CYC} limits are given in section 6.2

14.OSCILLATOR CIRCUIT

The SED1335 series incorporates an oscillator circuit. A stable oscillator can be constructed simply by connecting an AT-cut crystal and two capacitors to XG and XD, as shown in the figure below. If the oscillator frequency is increased, C_D and C_G should be decreased proportionally.

Note that the circuit board lines to XG and XD must be as short as possible to prevent wiring capacitance from changing the oscillator frequency or increasing the power consumption .



$C_D = 3$ to 20 pF

$C_G = 2$ to 18 pF

Load impedance = 700 ohm (max)

Figure 40. Crystal Oscillator

15.STATUS FLAG

The SED1335 series has a single bit status flag.

D7							D0
X	D6	X	X	X	X	X	X

X: Don't care

Figure 41. Status flag

The D6 status flag is HIGH for the TC/R-C/R cycles at the end of each line where the SED1335 series is not reading the display memory . The microprocessor may use this period to update display memory without affecting the display, however it is recommended that the display be turned off when refreshing the whole display .

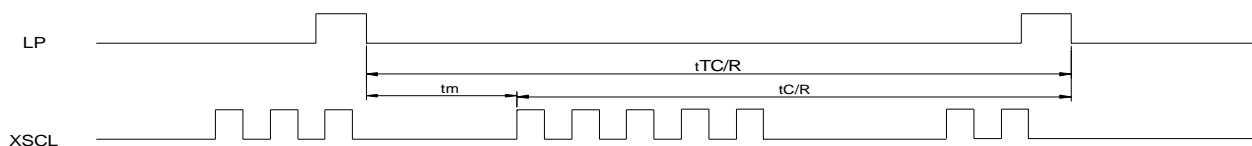


Figure 42 C/R to TC/R time difference

(CONTINUED)

/CS	A0	/RD	D6 (flag)
0	0	0	0: Period of retrace lines
			1: Period or display

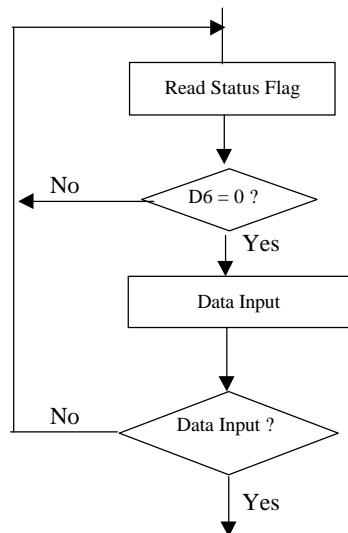
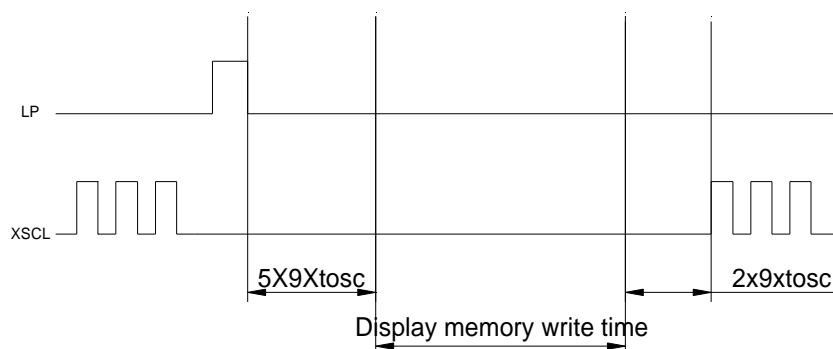


Figure 43. Flowchart for busy flag checking

< Timing To Be Observed For Avoiding SED 1330 Series Write Nois >

***Precaution on the write timing to VRAM**

The allowable writing duration is since "5 x 9 x tosc" has elapsed (tosc = 1/fOSC: a cycle of the oscillation frequency) from the positive going edge of LP up to $\{(TCR) - (C/R) - 7\} \times 9 \times tosc$

Currently employed D₆ status flag reading method does not identify the timing when the read D₆ = Low took place. Thus, negative going edge of LP should be used as the interrupt signal when implementing the writing in above timing. If you try to access the display memory in other timing than the above, flickering of the display screen will result .

16 . RESET

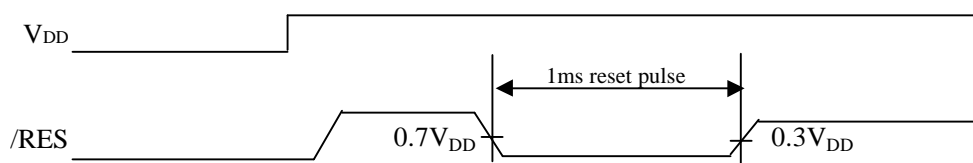


Figure 44. Reset timing

The SED1335 series requires a reset pulse at least 1 ms long after power-on in order to re-initialize its internal state .

For maximum reliability , it is not recommended to apply a DC voltage to the LCD panel while the SED1335 series is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse. The SED1335 series cannot receive commands while it is reset. Commands to initialize the internal registers should be issued soon after a reset .

During reset, the LCD drive signals XD, LP and FR are halted .

A delay of 3 ms (maximum) is required following the rising edges of both /RES and VDD to allow for system stabilization .

17 . APPLICATION NOTES

Initialization Parameters

The parameters for the initialization commands must be determined first. Square brackets around a parameter name indicate the number represented by the parameter, rather than the value written to the parameter register. For example , $[FX] = FX + 1$

SYSTEM SET instruction and parameters

* FX

The horizontal character field size is determined from the horizontal display size in pixels [VD] and the number of characters per line [VC] .

*C/R

C/R can be determined from VC and FX .

where $RND_{(x)}$ denotes x rounded up to the next highest integer. [C/R] is the number of bytes per line, not the number of characters .

*TC/R

TC/R must satisfy the condition $[TC/R] = [C/R] + 4$.

*f_{OSC} and f_{FR}

Once TC/R has been set, the frame frequency, f_{FR} , and lines per frame [L/F] will also have been set. The lower limit on the oscillator frequency f_{OSC} is given by : $f_{OSC} = ([TC/R] \times 9 + 1) \times [L/F] \times f_{FR}$

* If no standard crystal close to the calculated value of f_{OSC} exists, a higher frequency crystal can be used and the value of TC/R revisited using the above equation .

*Symptoms of an incorrect TC/R setting are listed below. If any of these appears check the value of TC/R and modify it if necessary .

- Vertical scanning halts and a high-contrast horizontal line appears.
- All pixels are on or off.
- The LP output signal is absent or corrupted.
- The display is unstable .

18. LCD Modules Handling precautions

- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place ,etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out , do not get any in your mouth . If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. handle this polarize carefully
- To prevent destruction of the elements by static electricity , be careful to maintain an optimum work environment.
 - Be sure to ground the body when handling the LCD Modules.
 - Tools required for assembly, such as soldering irons, must be properly grounded.
 - To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
 - The LCD Module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage Precautions

When storing the LCD Modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C).Whenever possible, the LCD Modules should be stored in the same conditions in which they were shipped from our company.

19. Others

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- If the LCD Modules have been operating for a long time showing the same display patterns the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time.
It should be noted that this phenomena does not adversely affect performance reliability.
- To minimize the performance degradation of the LCD Modules resulting from caused by static electricity , etc . Exercise care to avoid holding the following sections when handling the modules:
 - Exposed area of the printed circuit board
 - Terminal electrode sections