ALPHA & OMEGA SEMICONDUCTOR

AOD4189

P-Channel Enhancement Mode Field Effect Transistor

General Description

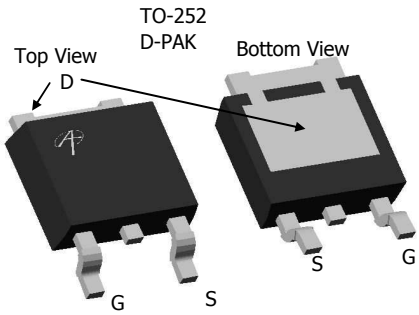
The AOD4189 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications.

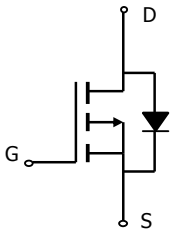
-RoHS Compliant
-Halogen Free*

Features

V_{DS} (V) = -40V
I_D = -40A (V_{GS} = -10V)
$R_{DS(ON)}$ < 22mΩ (V_{GS} = -10V)
$R_{DS(ON)}$ < 29mΩ (V_{GS} = -4.5V)

100% UIS Tested!
100% Rg Tested!





Absolute Maximum Ratings T_C=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [B,H]	T_C=25°C	I_D	-40	A
	T_C=100°C		-28	
Pulsed Drain Current [C]		I_{DM}	-50	
Avalanche Current [C]		I_{AR}	-35	
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	61	mJ
Power Dissipation [B]	T_C=25°C	P_D	62.5	W
	T_C=100°C		31	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.5	
	T_A=70°C		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A,G]	t ≤ 10s	$R_{\theta JA}$	15	20	°C/W
Maximum Junction-to-Ambient [A,G]	Steady-State		41	50	°C/W
Maximum Junction-to-Case [D,F]	Steady-State	$R_{\theta JC}$	2	2.4	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-40V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1.7	-1.9	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-50			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-12A		18	22	mΩ
		T_J=125°C		27	33	
		V_{GS}=-4.5V, I_D=-8A		23	29	
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-12A		35		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.74	-1	V
I_S	Maximum Body-Diode Continuous Current				-20	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-20V, f=1MHz		1870		pF
C_{oss}	Output Capacitance			185		pF
C_{rss}	Reverse Transfer Capacitance			155		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	2.5	4.5	6.5	Ω
SWITCHING PARAMETERS						
Q_g (-10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-20V, I_D=-12A		31.4	41	nC
Q_g (-4.5V)	Total Gate Charge			7.9	10	
Q_{gs}	Gate Source Charge			7.6		nC
Q_{gd}	Gate Drain Charge			6.2		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-20V, R_L=1.6Ω, R_{GEN}=3Ω		10		ns
t_r	Turn-On Rise Time			18		ns
$t_{D(off)}$	Turn-Off DelayTime			38		ns
t_f	Turn-Off Fall Time			24		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-12A, dI/dt=100A/µs		32	42	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-12A, dI/dt=100A/µs		30		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25°C. The power dissipation P_{DSM} and current rating I_{DSM} are based on $T_{J(MAX)}$=150°C, using steady state junction-to-ambient thermal resistance.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using t ≤300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

H. The maximum current rating is limited by bond-wires.

*This device is guaranteed green after data code 8X11 (Sep 1 ST 2008).

Rev1: Oct 2008

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

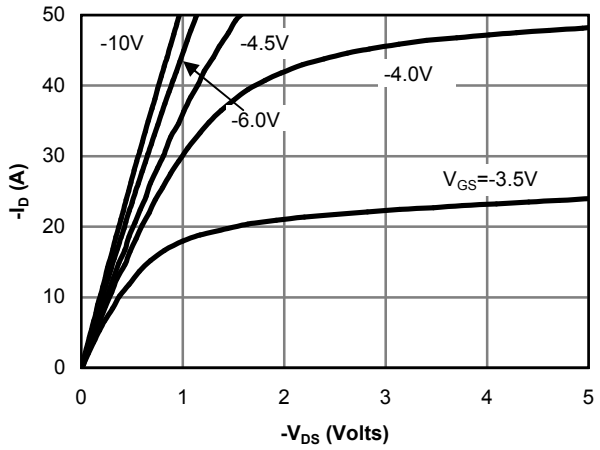


Figure 1: On-Region Characteristics

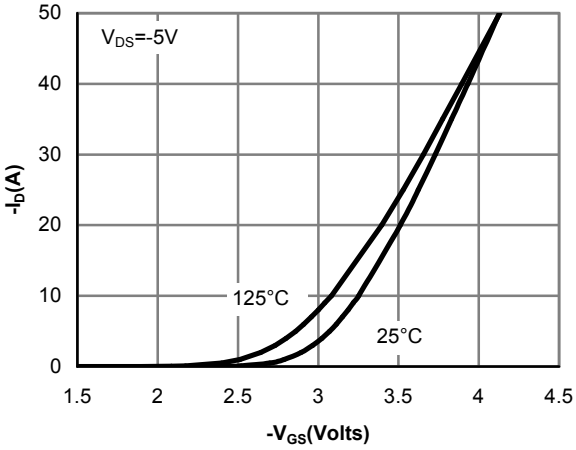


Figure 2: Transfer Characteristics

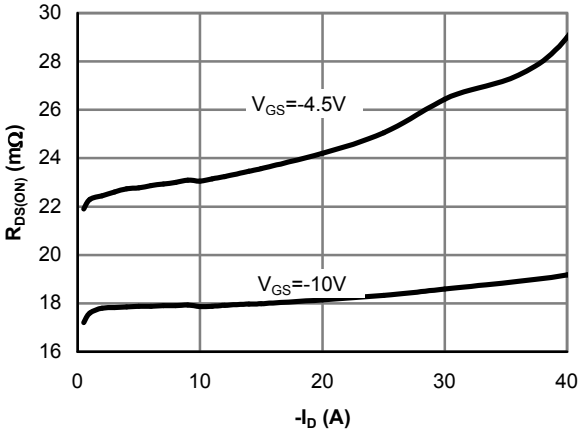


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

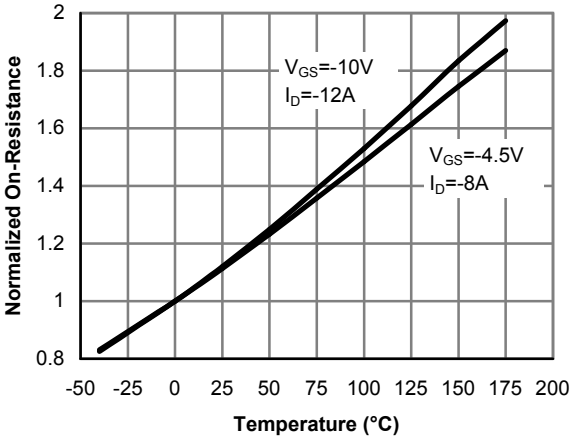


Figure 4: On-Resistance vs. Junction Temperature

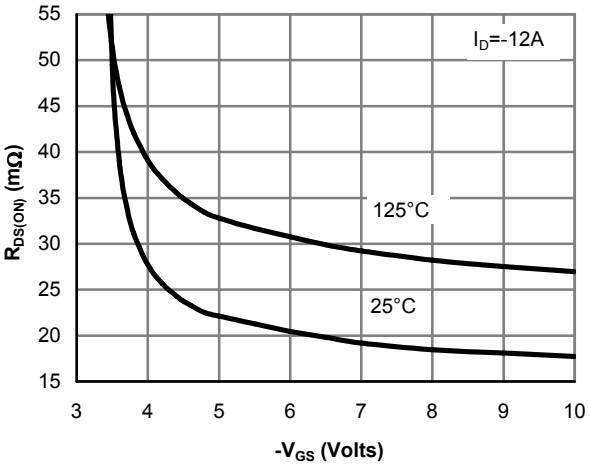


Figure 5: On-Resistance vs. Gate-Source Voltage

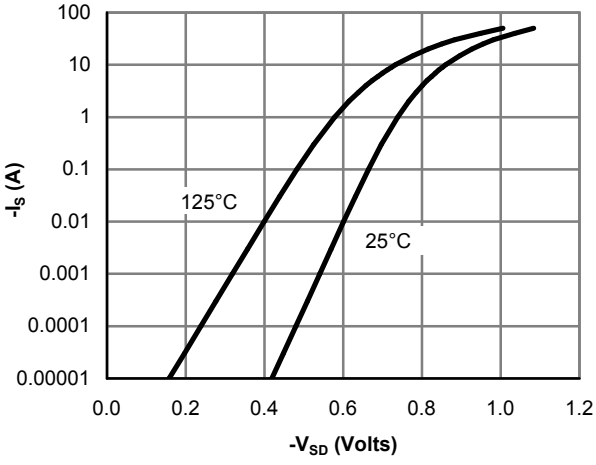


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

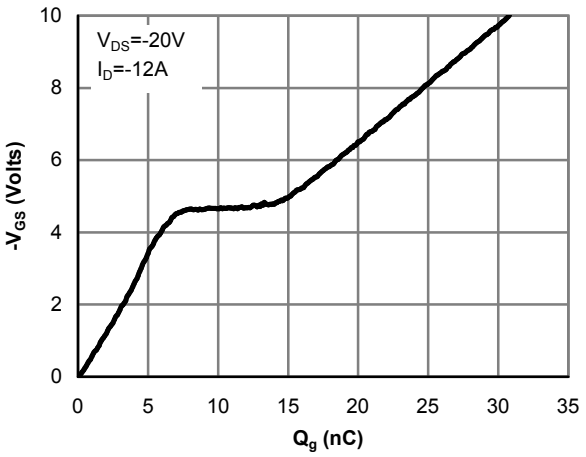


Figure 7: Gate-Charge Characteristics

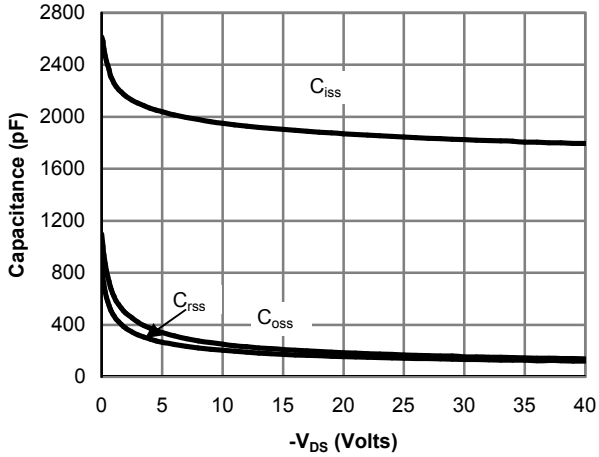


Figure 8: Capacitance Characteristics

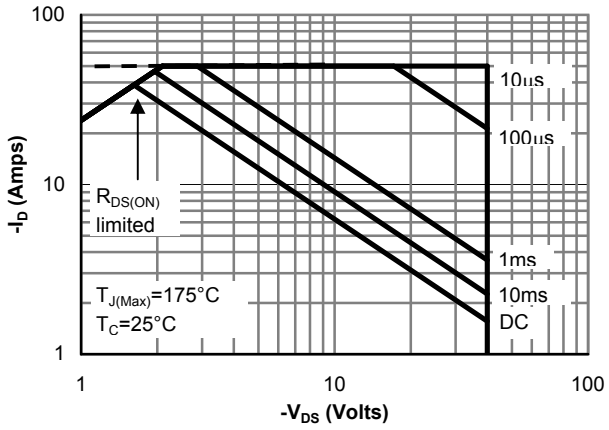


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

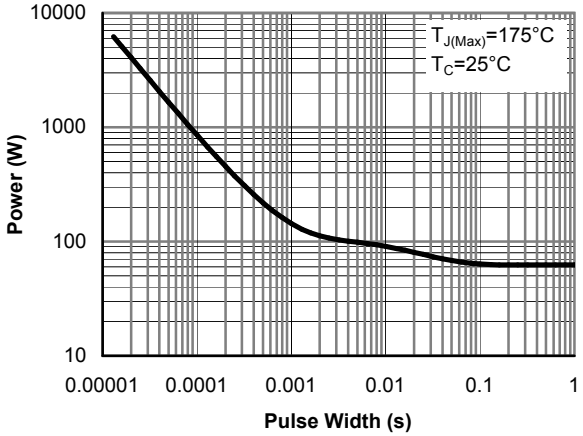


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

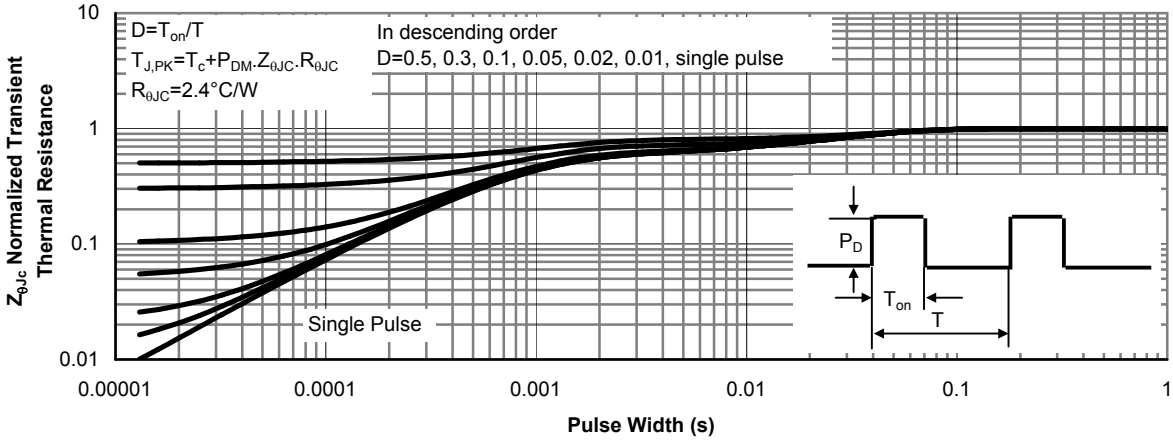


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

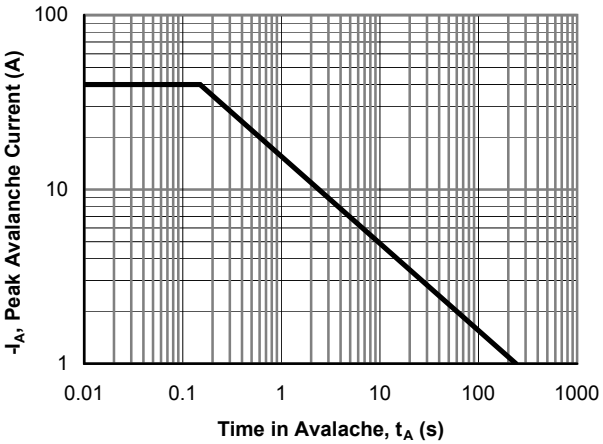


Figure 12: Single Pulse Avalanche Capability

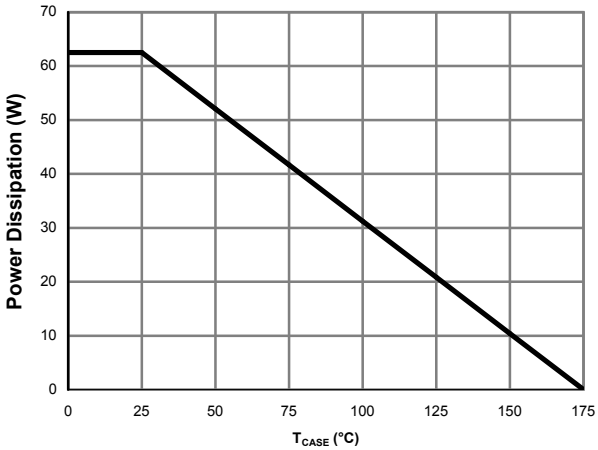


Figure 13: Power De-rating (Note B)

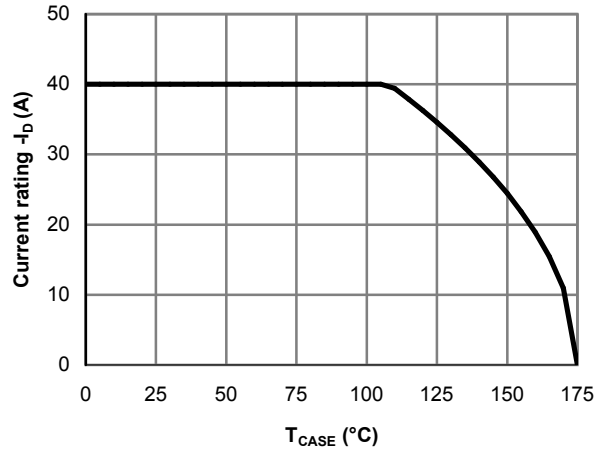


Figure 14: Current De-rating (Note B)

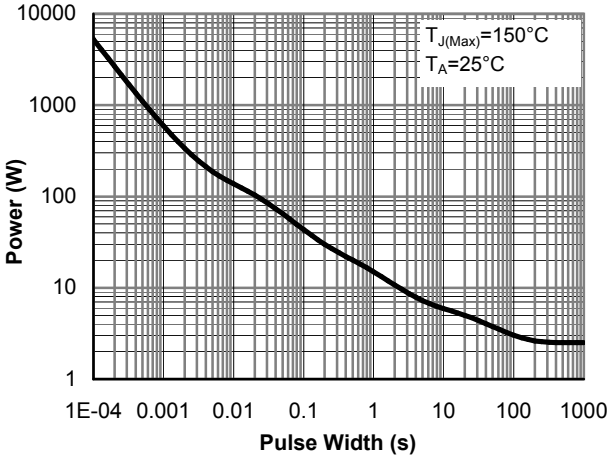


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

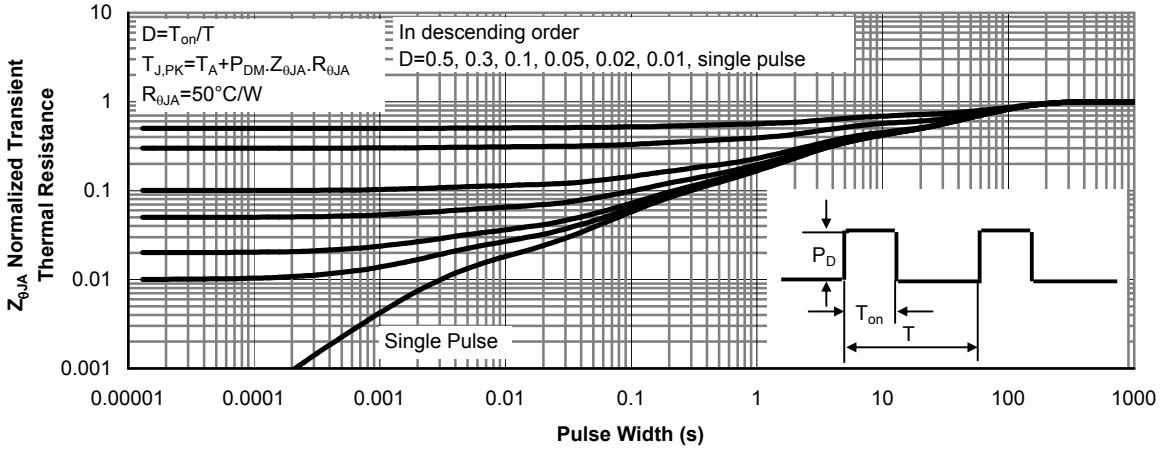
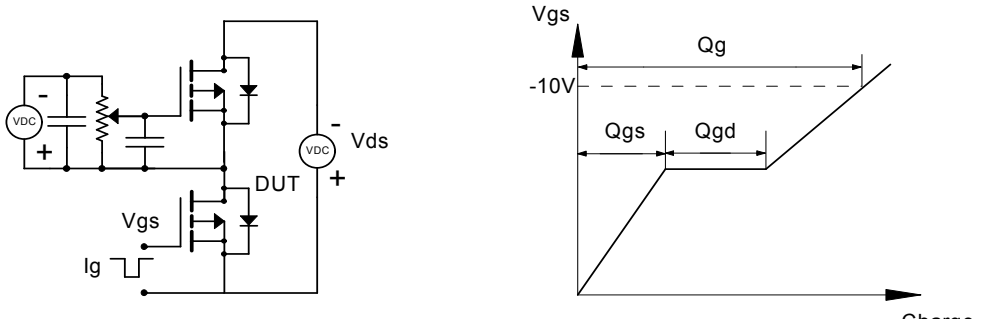
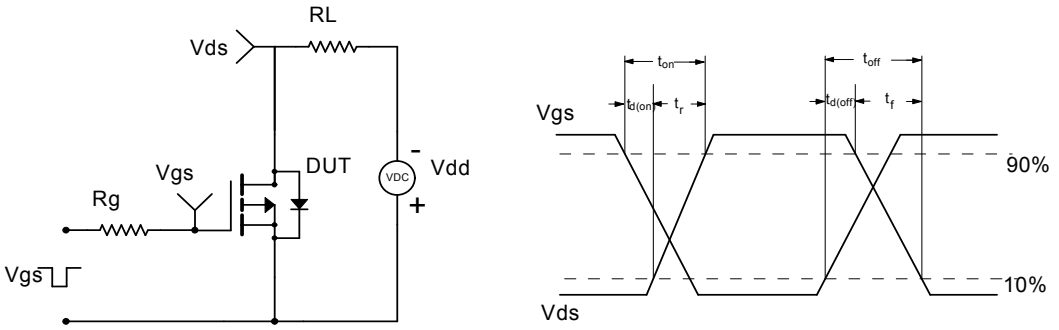


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

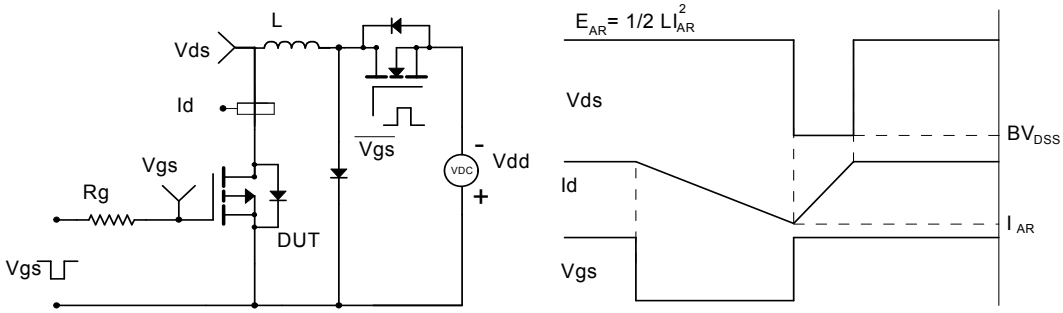
Gate Charge Test Circuit & Waveform



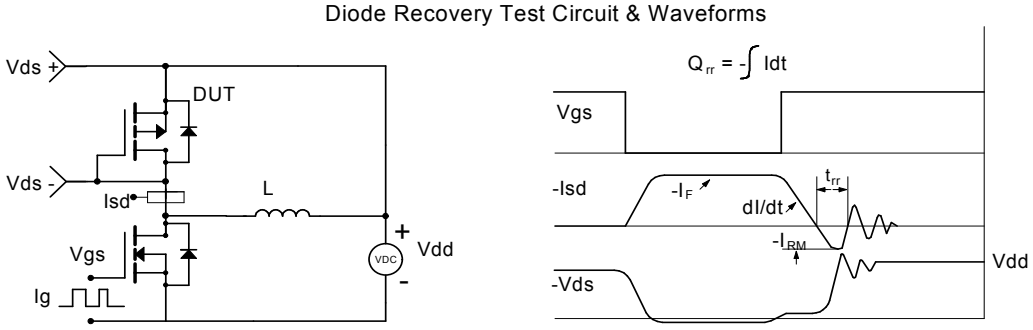
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



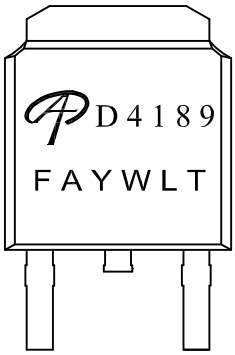
Diode Recovery Test Circuit & Waveforms



ALPHA & OMEGA SEMICONDUCTOR

Document No.	PD-00622
Version	C
Title	AOD4189 Marking Description

DPAK PACKAGE MARKING DESCRIPTION



Green product

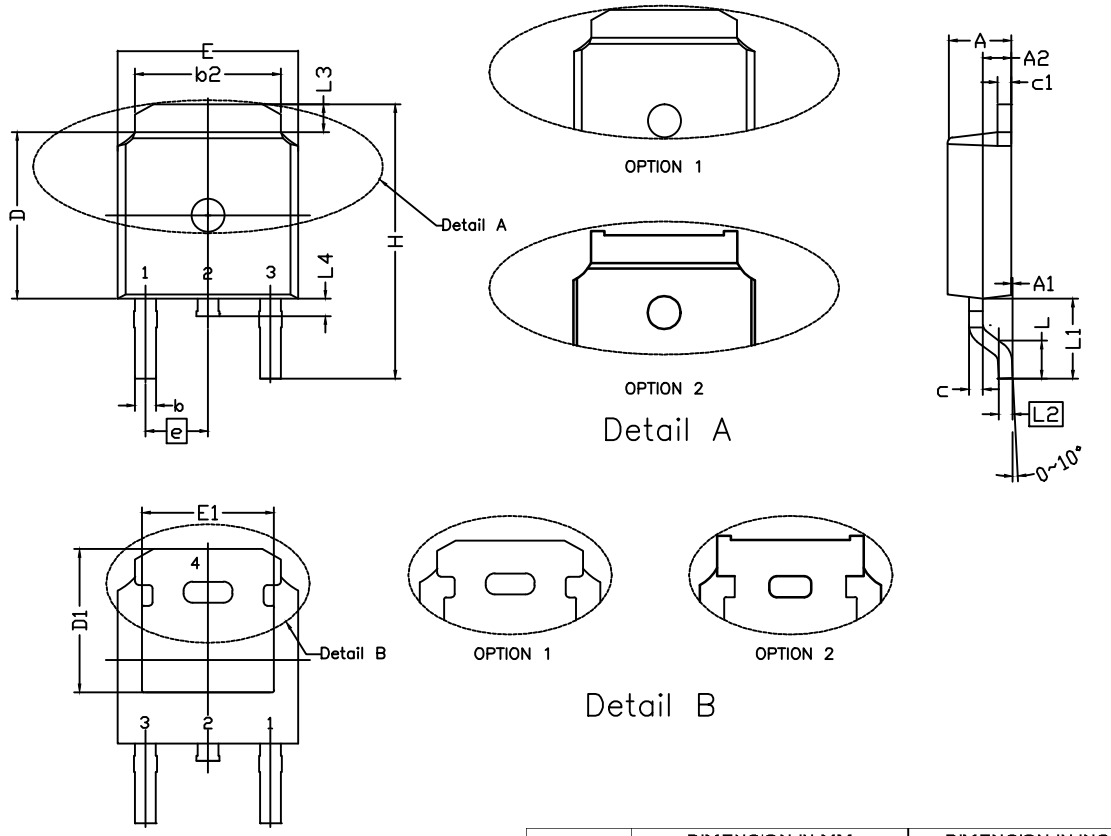
NOTE:
LOGO - AOS Logo
D4189 - Part number code
F - Fab code
A - Assembly location code
Y - Year code
W - Week code
L&T - Assembly lot code

PART NO.	DESCRIPTION	CODE
AOD4189	Green product	D4189
AOD4189L	Green product	D4189

ALPHA & OMEGA
SEMICONDUCTOR, LTD.

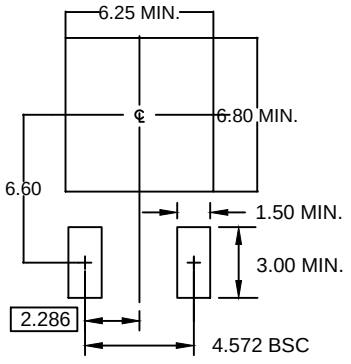
Document No.	PO−00009
Version	U

TO252 PACKAGE OUTLINE



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.184	2.286	2.400	0.086	0.090	0.094
A1	0.000	---	0.200	0.000	---	0.008
A2	0.889	1.041	1.170	0.035	0.041	0.046
b	0.635	0.762	0.889	0.025	0.030	0.035
b1	0.680	0.840	1.143	0.027	0.033	0.045
b2	4.953	5.340	5.500	0.195	0.210	0.217
c	0.450	0.508	0.610	0.018	0.020	0.024
c1	0.450	0.508	0.630	0.018	0.020	0.025
D	5.969	6.096	6.223	0.235	0.240	0.245
D1	5.210	5.249	5.380	0.205	0.207	0.212
E	6.350	6.604	6.800	0.250	0.260	0.268
E1	4.318	4.826	4.920	0.170	0.190	0.194
e	2.286 BSC			0.090 BSC		
e1	4.572 BSC			0.180 BSC		
H	9.398	10.033	10.500	0.370	0.395	0.413
L	1.270	1.520	2.032	0.050	0.060	0.080
L1	2.921 REF.			0.115 REF.		
L2	0.408	0.508	0.608	0.016	0.020	0.024
L3	0.889	1.016	1.270	0.035	0.040	0.050
L4	0.600	---	1.016	0.024	---	0.040

RECOMMENDED LAND PATTERN



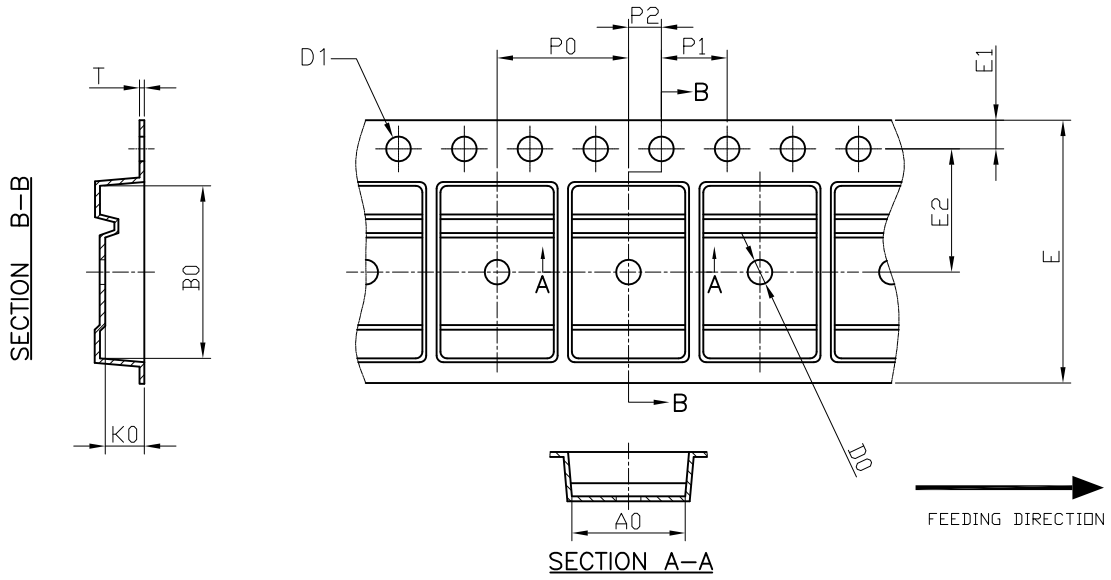
UNIT: mm

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MILS.
2. DIMENSION L IS MEASURED IN GAUGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-252 (AA)

ALPHA & OMEGA SEMICONDUCTOR

DPAK Tape and Reel Data

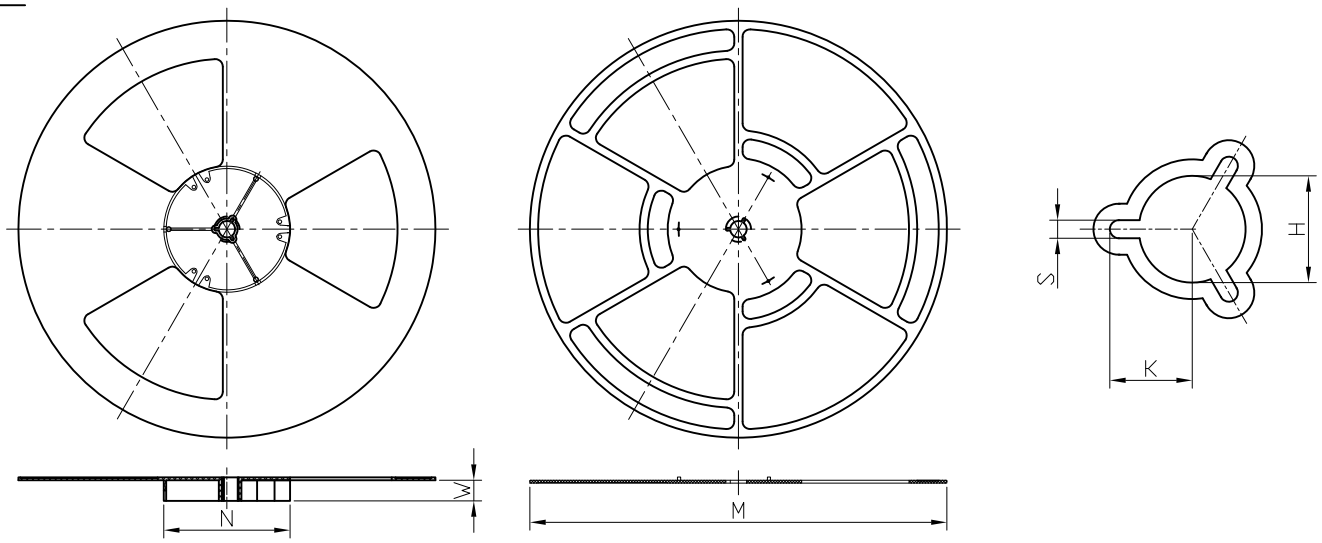
DPAK Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DPAK (16 mm)	6.90 ±0.10	10.50 ±0.10	2.50 ±0.10	1.50 +0.1 −0	1.50 +0.1 −0	16.00 ±0.30	1.75 ±0.10	7.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.30 ±0.05

DPAK Reel



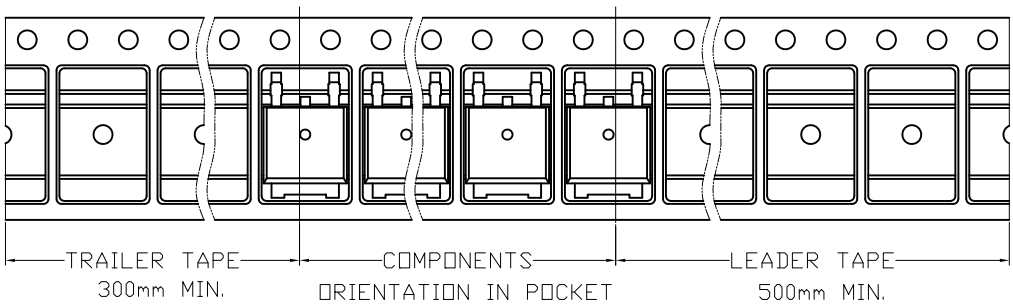
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	H	K	S
16 mm	ø330	ø330.00 +0.25 −4.00	ø100.00 ±0.2	16.4 +2.0 −0.0	ø13.00 +0.50 −0.20	10.5 ±0.25	2.2 ±0.25

DPAK Tape

Leader / Trailer & Orientation

Unit Per Reel: 2500pcs



AOS Semiconductor
Product Reliability Report

AOD4189, rev D

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

Jun, 2018

ALPHA & OMEGA SEMICONDUCTOR

This AOS product reliability report summarizes the qualification result for AOD4189. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AOD4189 passes AOS quality and reliability requirements. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTGB	Temp = 150°C , Vgs=100% of Vgsmax	168 / 500 / 1000 hours	924 pcs	0	JESD22-A108
HTRB	Temp = 150°C , Vds=80% of Vdsmax	168 / 500 / 1000 hours	924 pcs	0	JESD22-A108
Precondition (Note A)	168hr 85°C / 85%RH + 3 cycle reflow@260°C (MSL 1)	-	4620 pcs	0	JESD22-A113
HAST	130°C , 85%RH, 33.3 psia, Vds = 80% of Vdsmax	96 hours	693 pcs	0	JESD22-A110
H3TRB	85°C , 85%RH, Vds = 80% of Vdsmax	1000 hours	693 pcs	0	JESD22-A101
Autoclave	121°C , 29.7psia, RH=100%	96 hours	924 pcs	0	JESD22-A102
Temperature Cycle	-65°C to 150°C , air to air,	1000cycles	924 pcs	0	JESD22-A104
HTSL	Temp = 150°C	1000 hours	693 pcs	0	JESD22-A103
IOL	Δ Tj = 100°C	15000 cycles	693 pcs	0	MIL-STD-750 Method 1037

Note: The reliability data presents total of available generic data up to the published date.
Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

FIT rate (per billion): 1.91
MTTF = 59839 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 \times 10^9$ **/ [**2 (N) (H) (Af)**] =** 1.91
MTTF = 10^9 / FIT =59839 years
Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from burn-in tests
H = Duration of burn-in testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)
Acceleration Factor [**Af**] = **Exp** [Ea / **k** (1/Tj u – 1/Tj s)]

Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	259	87	32	13	5.64	2.59	1

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16
Tj u =The use junction temperature in degree (Kelvin), K = C+273.16
k = Boltzmann's constant, 8.617164 X 10^{-5}eV / K