MPQ4313

45V, 3A, Low I_Q Synchronous Step-Down Converter with Frequency Spread Spectrum, AEC-Q100 Qualified

DESCRIPTION

The MPQ4313 is a frequency-programmable, synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFET. It provides up to 3A of highly efficient output, with current mode control for fast loop response.

The wide 3.3V to 45V input voltage range accommodates a variety of step-down applications in an automotive input environment. A 1.7μA shutdown mode quiescent current allows the part to be used in battery-powered applications. High power conversion efficiency over a wide load range is achieved by scaling down the switching frequency in light-load conditions to reduce the switching and gate driver losses.

An open-drain power good signal indicates whether the output is within 95% to 105% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. High-duty cycle and low-dropout mode are provided for automotive cold crank conditions.

The MPQ4313 is available in a QFN-20 (4mmx4mm) package.

MPQ4313 FAMILY VERSIONS

Part Number	Output Current	Package Options
MPQ4312	2A	QFN-20 (4mmx4mm) WF (1)
MPQ4313	3A	
MPQ4314	4A	
MPQ4315	5A	
MPQ4316	6A	
MPQ4317	7A	

Note:

1) "WF" means wettable flank.

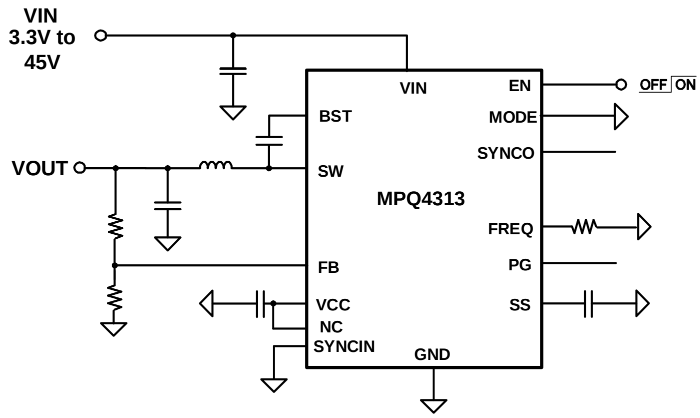
FEATURES

- Wide 3.3V to 45V Operating Range
- 3A Continuous Output Current
- 1.7μA Low Shutdown Supply Current
- 18μA Sleep Mode Quiescent Current
- Internal 48mΩ High-Side and 20mΩ Low-Side MOSFETs
- 350kHz to 530kHz Programmable Switching Frequency for Car Battery Applications
- Switching Frequency Can Be Synchronized to External Clock
- Out-of-Phase Synchronized Clock Output
- 3.3V, 5V Fixed Output Options
- Frequency Spread Spectrum (FSS) for Low EMI
- Symmetric V_{IN} for Low EMI
- Power Good Output
- External Soft Start
- 100ns Minimum On Time
- Selectable Advanced Asynchronous Mode (AAM) or Forced Continuous Conduction Mode (FCCM)
- Low-Dropout Mode
- Hiccup Over-Current Protection
- Available in a QFN-20 (4mmx4mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

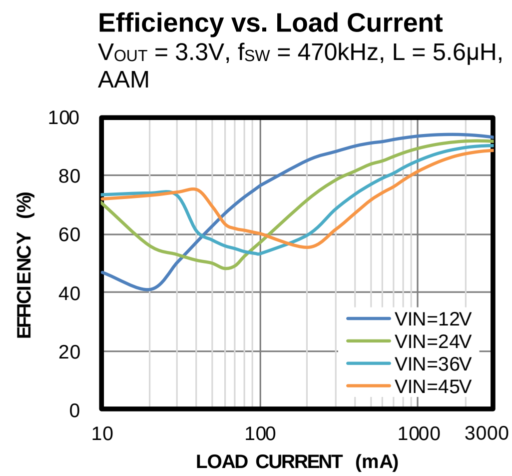
APPLICATIONS

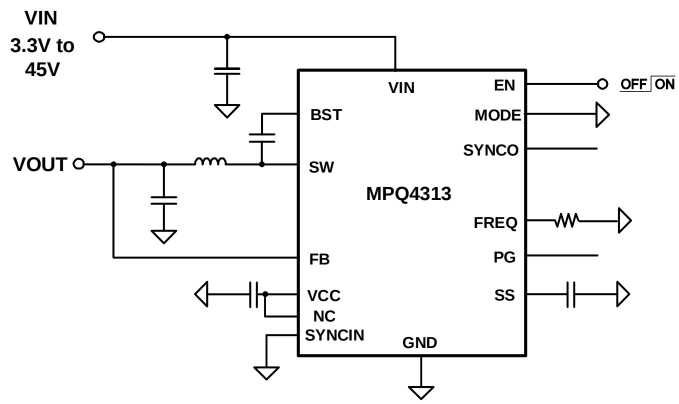
- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems
- Industrial Power Systems

TYPICAL APPLICATION



Adjustable Output Version





Fixed Output Version

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4313GRE-AEC1***	QFN-20 (4mmx4mm)	*See Below*	1
MPQ4313GRE-33-AEC1***			
MPQ4313GRE-5-AEC1***			

* For Tape & Reel, add suffix –Z (e.g. MPQ4313GRE-AEC1–Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

TOP MARKING (MPQ4313GRE-AEC1)

<u>MPSYWW</u>
MP4313
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4313: Part number
LLLLLL: Lot number
E: Wettable flank

TOP MARKING (MPQ4313GRE-33-AEC1)

<u>MPSYWW</u>
MP4313
LLLLLL
E33

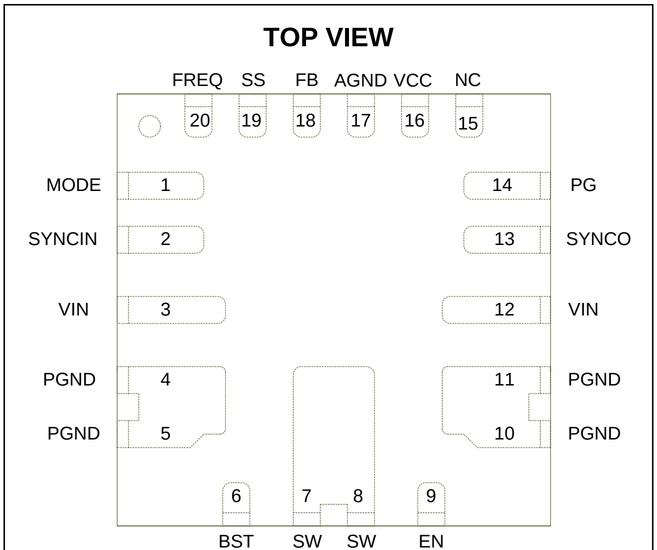
MPS: MPS prefix
Y: Year code
WW: Week code
MP4313: Part number
LLLLLL: Lot number
E: Wettable flank
33: 3.3V output

TOP MARKING (MPQ4313GRE-5-AEC1)

MPSYWW
MP4313
LLLLLL
E5

MPS: MPS prefix
Y: Year code
WW: Week code
MP4313: Part number
LLLLLL: Lot number
E: Wettable flank
5: 5V output

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**AAM or FCCM selection pin.** Pull this pin high to put the part in FCCM, and pull it low for AAM at light-load. Do not leave this pin floating.
2	SYNCIN	**SYNC input.** Apply a 350kHz to 530kHz clock signal to this pin to synchronize the internal oscillator frequency to the external clock. This pin is also used for multi-phase operation. Connect SYNCIN to GND if not used; do not float this pin.
3, 12	VIN	**Input supply.** VIN supplies power to all the internal control circuitry and the power switch connected to SW. A decoupling capacitor to ground is recommended to be placed close to VIN to minimize switching spikes.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between this BST and SW.
7, 8	SW	**Switch node.** SW is the output of the internal power switch.
9	EN	**Enable.** Pull this pin below the specified threshold (0.85V) to shut down the chip. Pull it above the specified threshold (1V) to enable the chip.
13	SYNCO	**SYNC output.** Output a clock signal to be 180° out-of-phase from the internal oscillator signal or to be opposite from the clock signal applied at the SYNCIN pin. Leave this pin floating if not used.
14	PG	**Power good indicator.** The output of PG is an open drain; if this pin is used, a pull-up resistor to the power source is required. It goes high if the output voltage is within 95% to 105% of the nominal voltage, and goes low if the output voltage is above 106.5% or below 93.5% of the nominal voltage.
15	NC	**Not connected.** Connect this pin to the VCC pin or V_{OUT}, which must be no less than 3V. Do not float this pin.
16	VCC	**Bias supply.** This supplies power to the internal control circuit and gate drivers. A decoupling capacitor to ground must be placed close to this pin. To calculate the size of this capacitor, see the Setting the VCC Capacitor section on page 32.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** For the adjustable output version, connect FB to the center point of the external resistor divider from the output to AGND to set the output voltage. The feedback threshold voltage is 0.815V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. For the fixed output version, connect the FB pin directly to the output.
19	SS	**Soft-start input.** Place a capacitor from SS to GND to set the soft-start period. The MPQ4313 sources 6µA from SS to the soft-start capacitor at start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during start-up.
20	FREQ	**Switching frequency program.** Connect a resistor from this pin to ground to set the switching frequency. To set the frequency, see the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics (TPC) section on page 14.

ABSOLUTE MAXIMUM RATINGS (2)

VIN, EN ....-0.3V to +50V
SW ....-0.3V to $V_{IN\ (MAX)}$ + 0.3V
BST .... V_{SW} + 6V
All other pins ....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (3) (5)
QFN-20 (4mmx4mm) 5.4W
Operating junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C

Electrostatic Discharge (ESD) Rating

Human body model (HBM)....................... ±2kV
Charged device model (CDM) .... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) ....3.3V to 45V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (4mmx4mm)
JESD51-7 (4).............................44.........9....°C/W
EVQ4313-R-00A (5)..................23.......2.5...°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on MPS standard EVB, 9cmx9cm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN UVLO rising threshold	IN_{UVLO_RISING}		2.8	3.0	3.2	V
VIN UVLO falling threshold	$IN_{UVLO\_FALLING}$		2.5	2.7	2.9	V
VIN UVLO hysteresis	IN_{UVLO_HYS}			280		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
VIN quiescent current	I_Q	FB = 0.85V, no load, sleep mode		18	26	µA
VIN quiescent current (switching) (6)	I_{Q_ACTIVE}	MODE = GND (AAM), switching, no load, R_{FB_UP} = 1MΩ, R_{FB_DOWN} = 316kΩ		20		µA
		MODE = high (FCCM), switching, f_{SW} = 2MHz, no load		40		mA
		MODE = high (FCCM), switching, f_{SW} = 470kHz, no load		9.5		mA
VIN shutdown current	I_{SHDN}	EN = 0V		1.7	2.5	µA
FB reference voltage	V_{FB}	V_{IN} = 3.3V to 45V, T_J = 25°C	807	815	823	mV
		V_{IN} = 3.3V to 45V	799	815	831	mV
Output voltage accuracy of MPQ4313-33	V_{OUT}	T_J = 25°C	3234	3300	3366	mV
			3201	3300	3399	mV
Output voltage accuracy of MPQ4313-5	V_{OUT}	T_J = 25°C	4900	5000	5100	mV
			4850	5000	5150	mV
FB current	I_{FB}	V_{FB} = 0.85V	-50	0	+50	nA
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
Minimum on time (6)	t_{ON_MIN}			100		ns
Minimum off time (6)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		530	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		SYNCIN or FREQ set switching frequency		180		deg
HS current limit (7)		Duty cycle = 30%	4.4	5.5	7.2	A
LS valley current limit	I_{LIMIT_VALLEY}		3.2	4	4.8	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ZCD current	I_{ZCD}	AAM	-0.15	0.1	+0.35	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM	2	4.5	7	A
Switch leakage current	I_{SW_LKG}			0.01	1	µA
HS switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		48	80	mΩ
LS switch on resistance	R_{ON_LS}	V_{CC} = 5V		20	40	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	4	6	8.5	µA
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			190		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE\_FALLING}$				0.4	V
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	92%	95%	98%	V_{REF}
		V_{FB} falling	102%	105%	108%	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	90.5%	93.5%	96.5%	
		V_{FB} rising	103.5%	106.5%	109.5%	
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising delay	$t_{PG\_R\_DELAY}$			35		µs
PG falling delay	$t_{PG\_F\_DELAY}$			35		µs
Thermal shutdown (6)	T_{SD}			170		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			20		°C

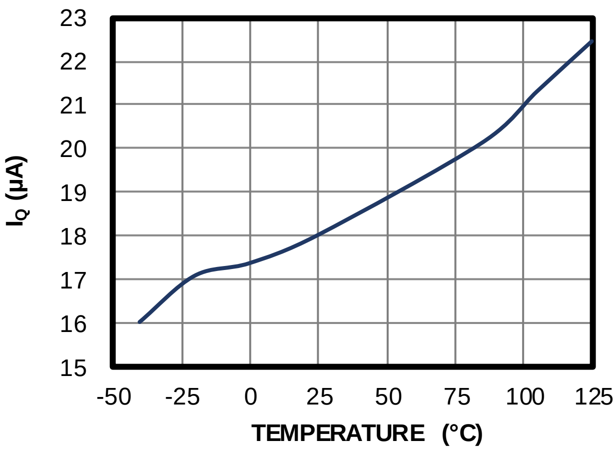
Notes:

6) Derived from bench characterization. Not tested in production.
7) Only guaranteed by characterization at T_J < 25°C. Not tested in production.

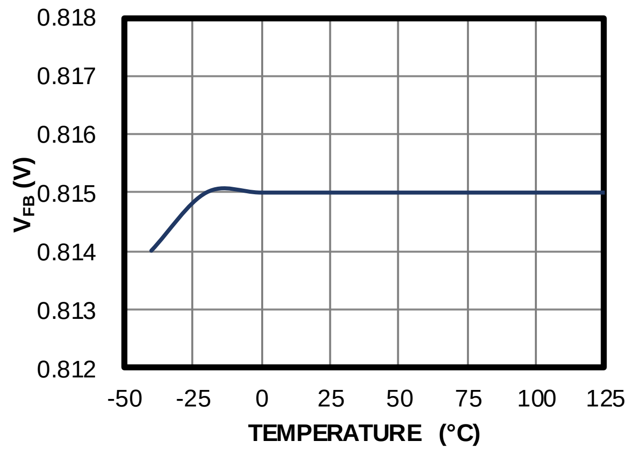
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

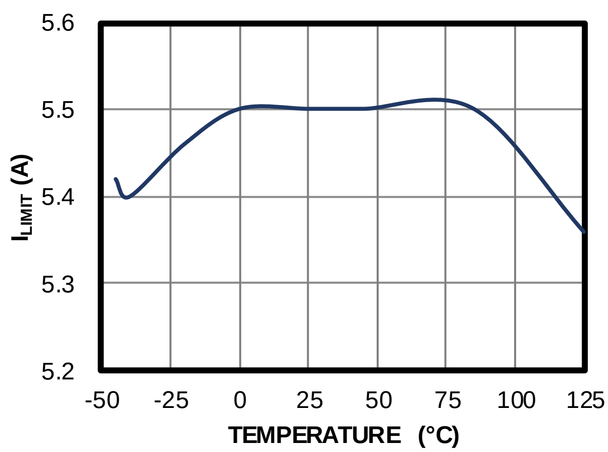
I_Q vs. Temperature



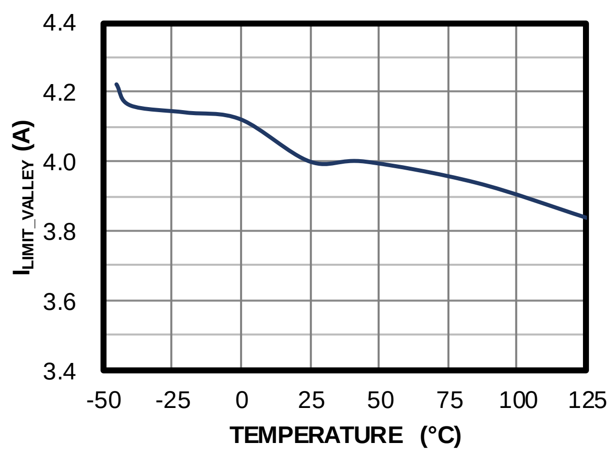
V_{FB} vs. Temperature



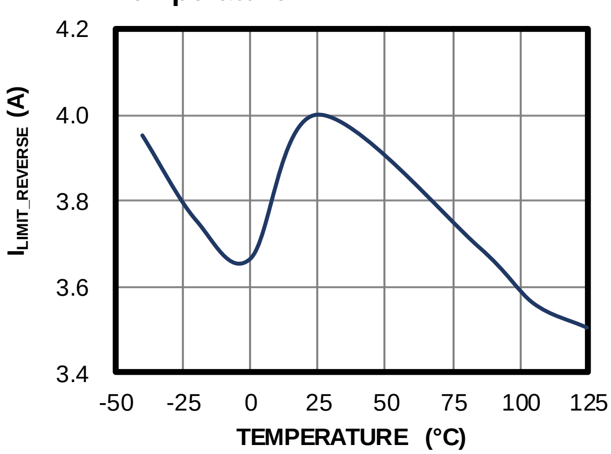
I_{LIMIT} vs. Temperature



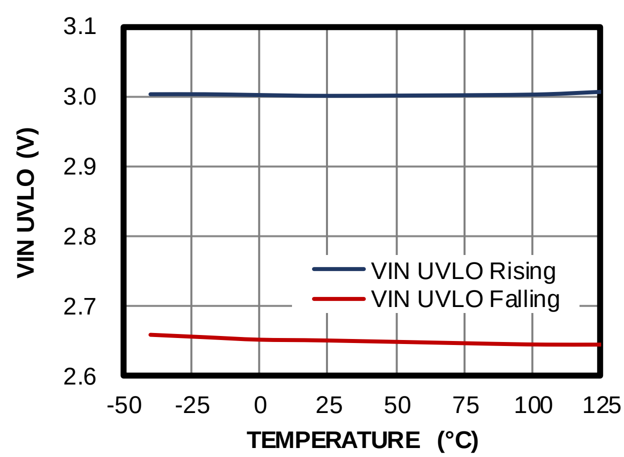
Valley Current Limit vs. Temperature



Reverse Current Limit vs. Temperature



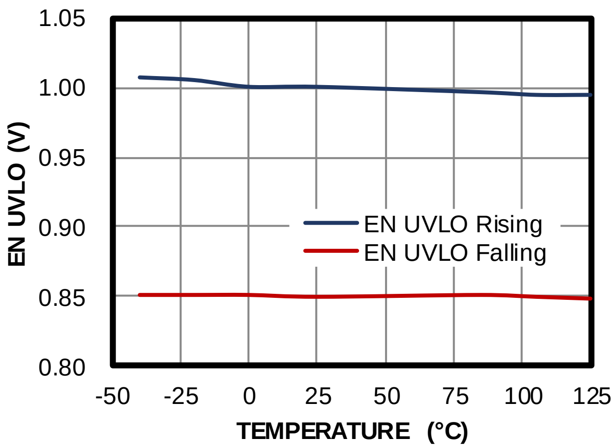
VIN UVLO Threshold vs. Temperature



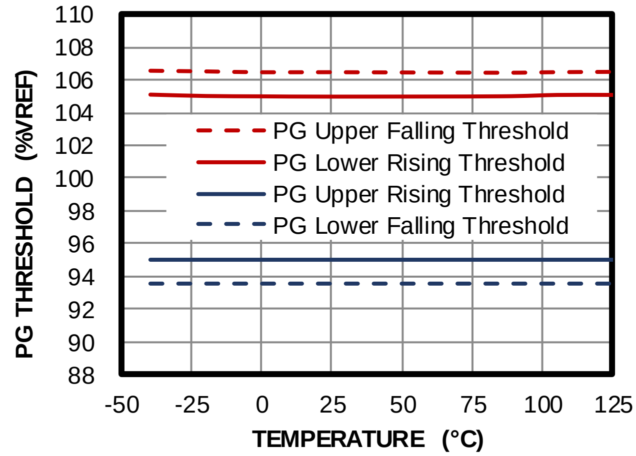
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

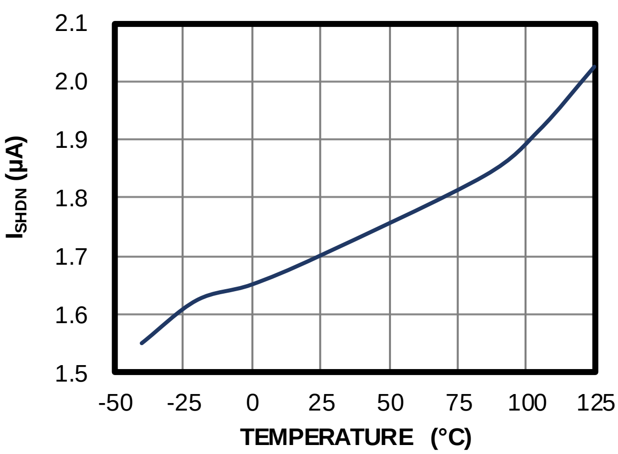
EN UVLO Threshold vs. Temperature



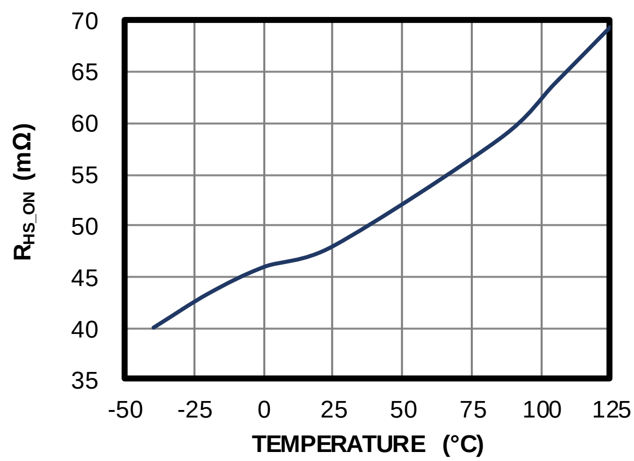
PG Rising/Falling Threshold vs. Temperature



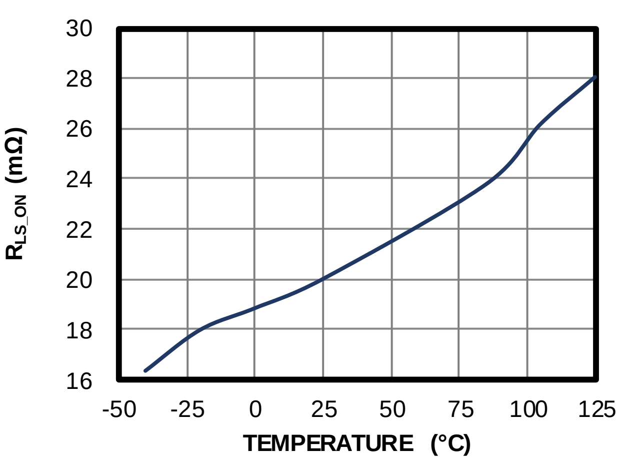
V_{IN} Shutdown Current vs. Temperature



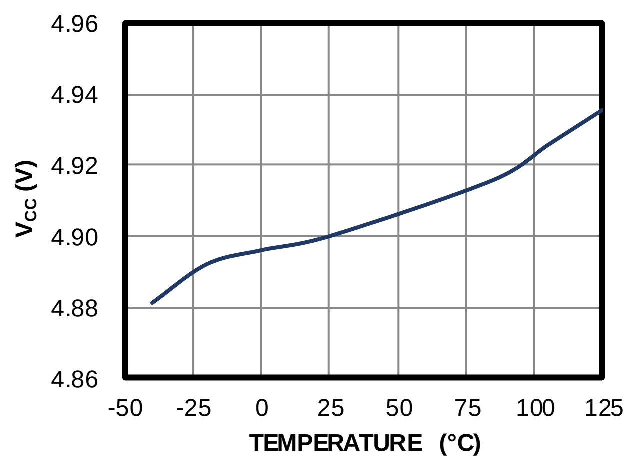
R_{HS_ON} vs. Temperature



R_{LS_ON} vs. Temperature



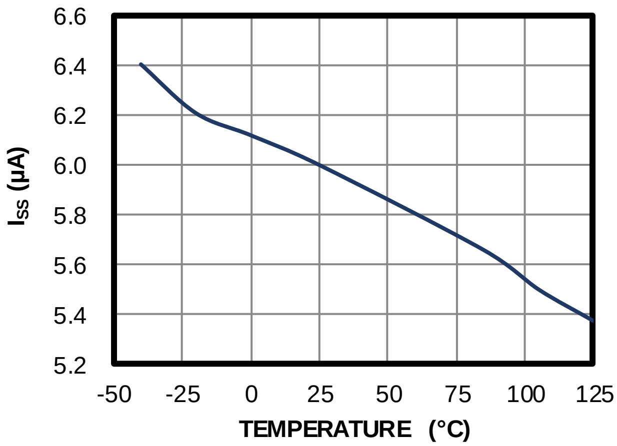
V_{CC} vs. Temperature



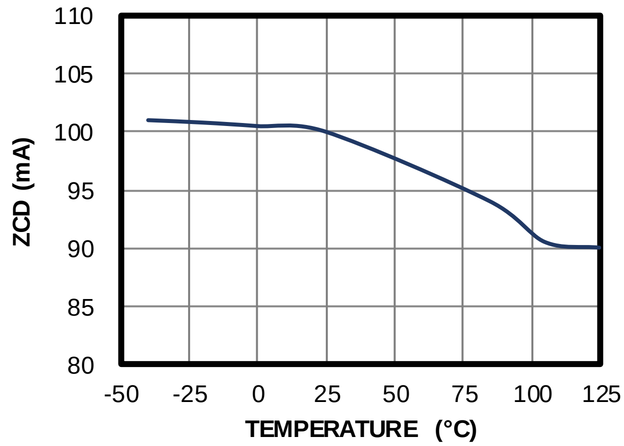
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Soft-Start Current vs. Temperature

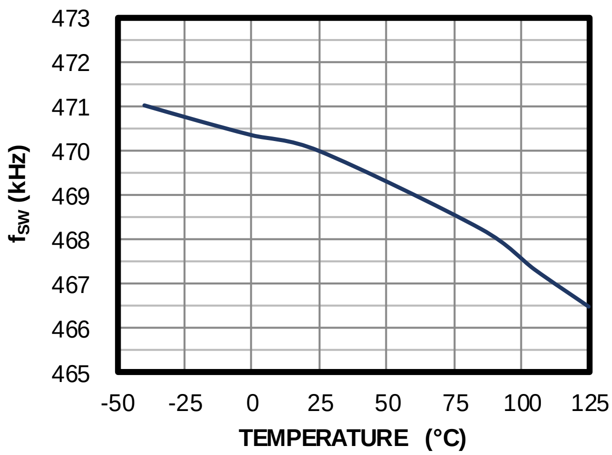


ZCD vs. Temperature



f_{SW} vs. Temperature

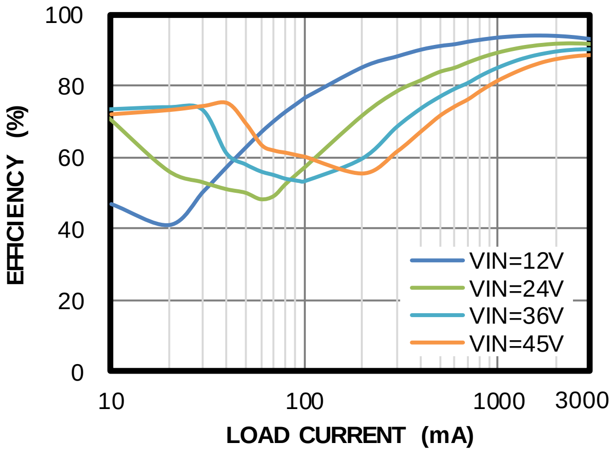
R_{FREQ} = 62kΩ



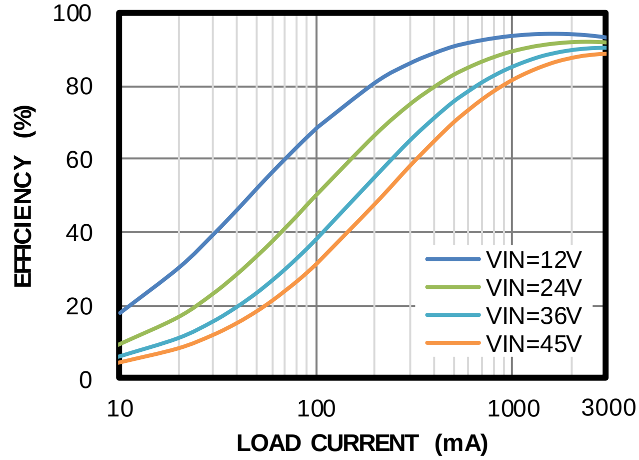
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, C_{OUT} = 94µF, f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted.

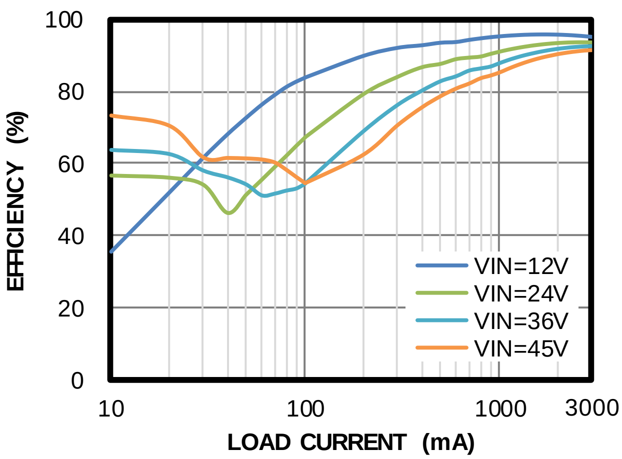
Efficiency vs. Load Current
AAM



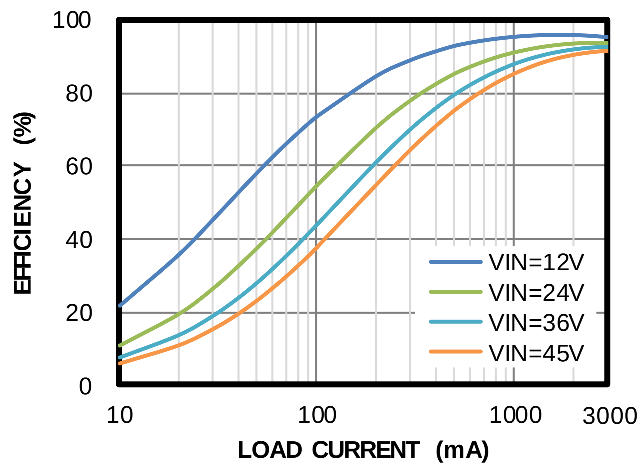
Efficiency vs. Load Current
FCCM



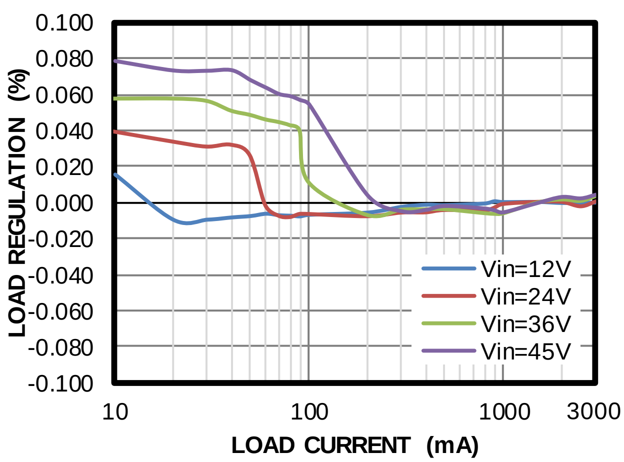
Efficiency vs. Load Current
AAM, V_{OUT} = 5V



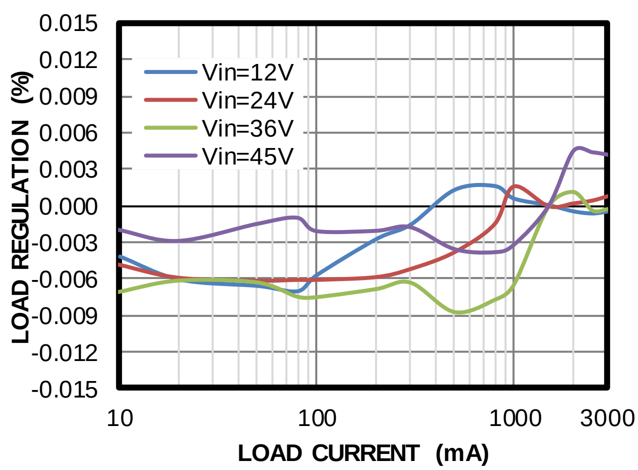
Efficiency vs. Load Current
FCCM, V_{OUT} = 5V



Load Regulation
AAM



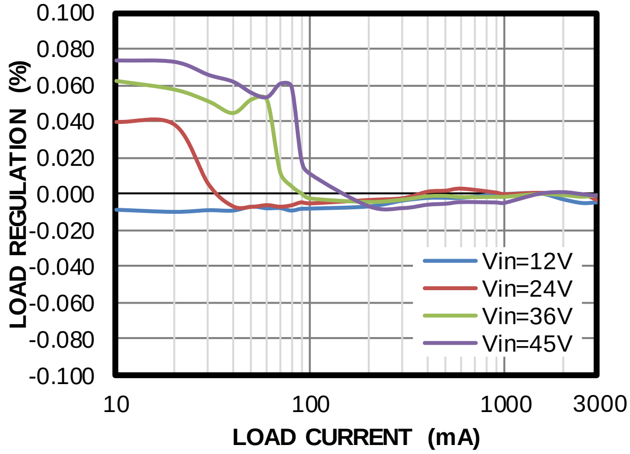
Load Regulation
FCCM



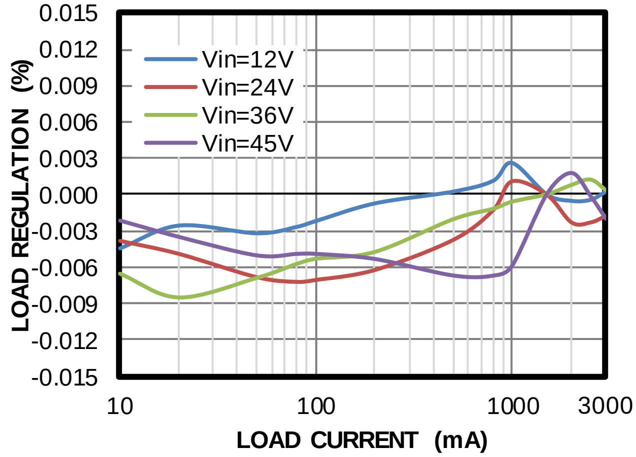
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, C_{OUT} = 94µF, f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted.

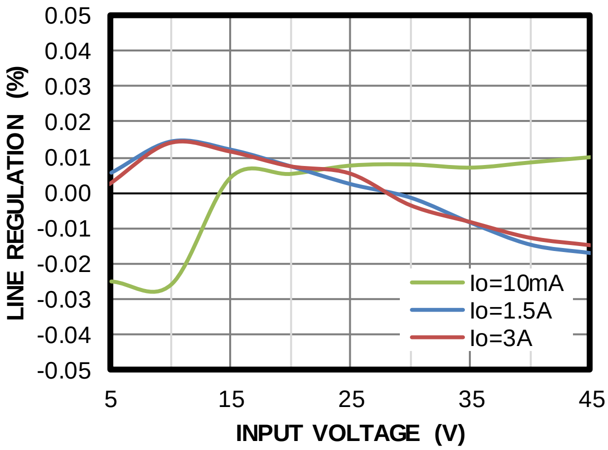
Load Regulation
AAM, V_{OUT} = 5V



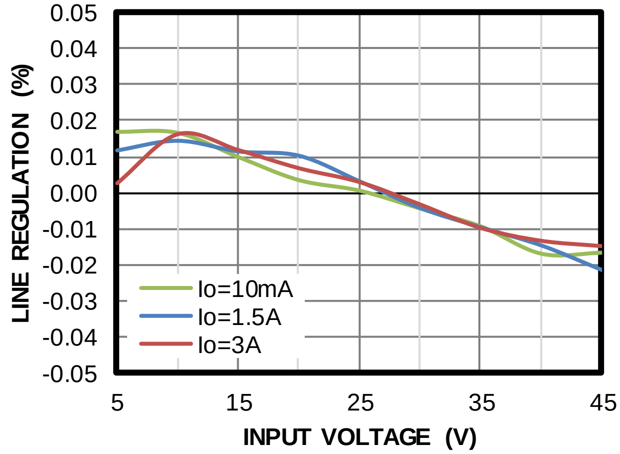
Load Regulation
FCCM, V_{OUT} = 5V



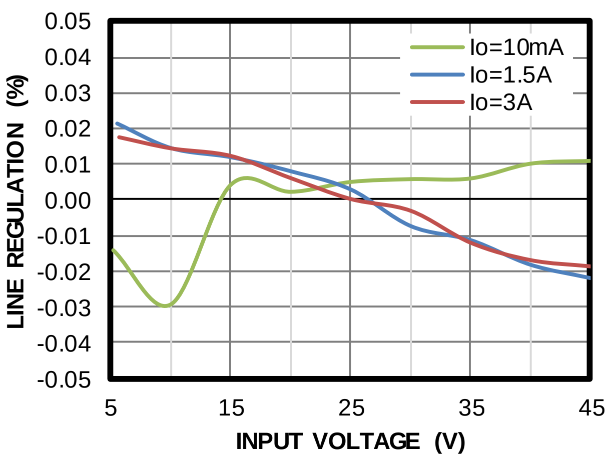
Line Regulation
AAM



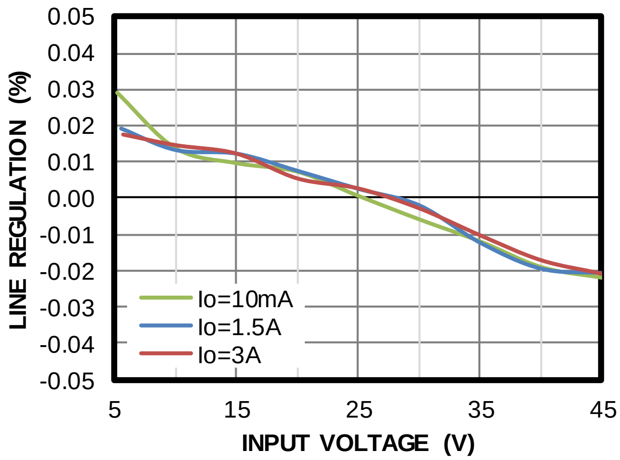
Line Regulation
FCCM



Line Regulation
AAM, V_{OUT} = 5V



Line Regulation
FCCM, V_{OUT} = 5V

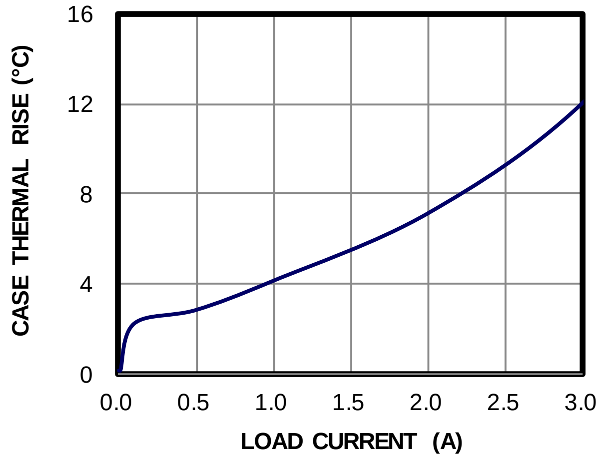


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, C_{OUT} = 94µF, f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted.

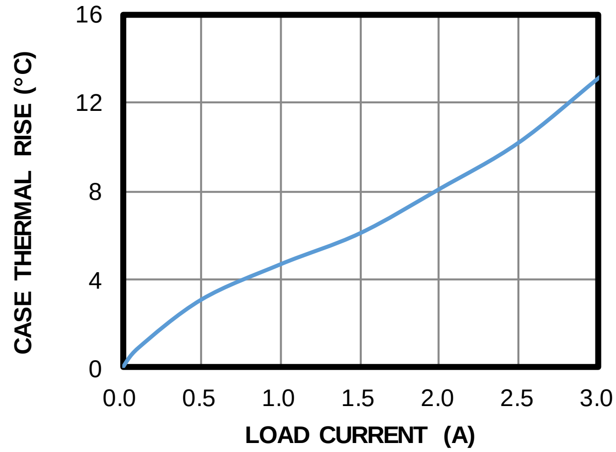
Case Thermal Rise

V_{OUT} = 3.3V

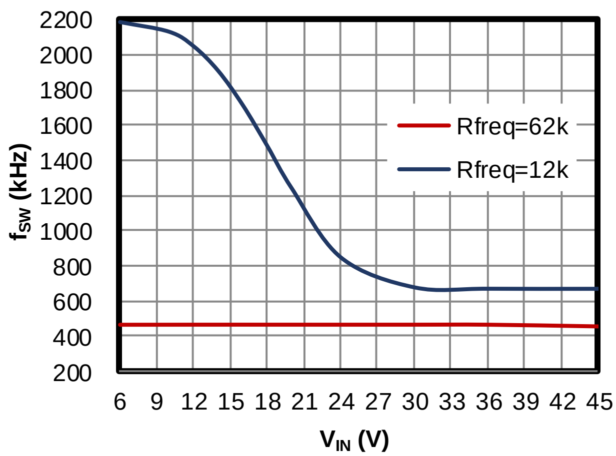


Case Thermal Rise

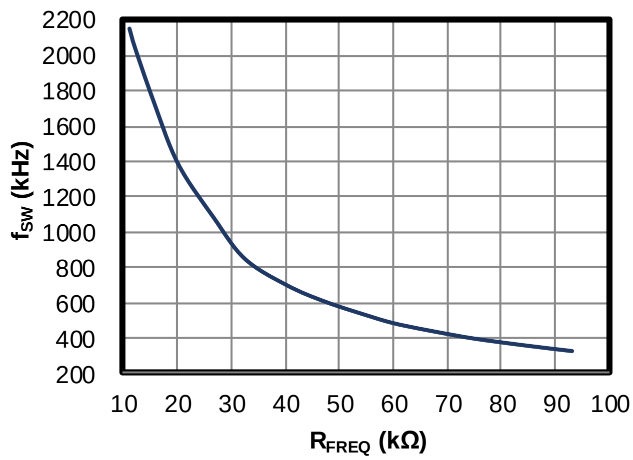
V_{OUT} = 5V



f_{SW} vs. V_{IN}

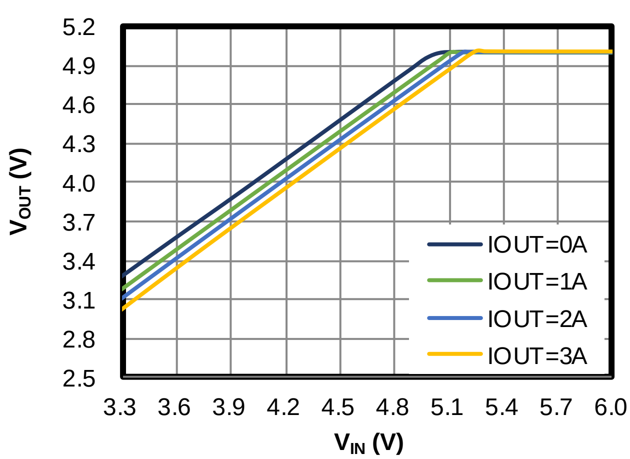


f_{SW} vs. R_{FREQ}



Low-Dropout Mode

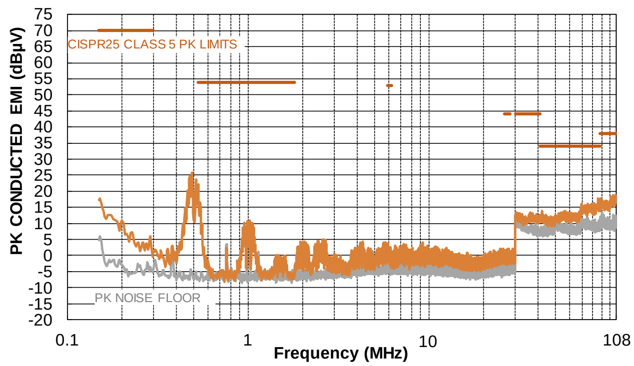
V_{OUT} = 5V



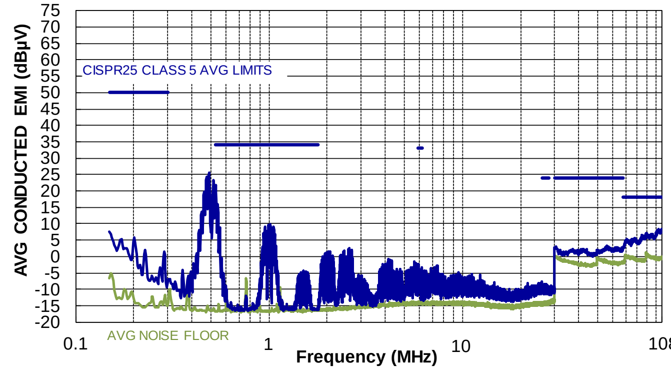
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, C_{OUT} = 94µF, f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted. (8)

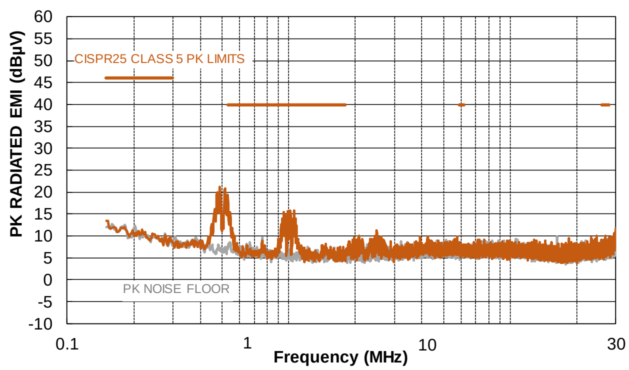
CISPR25 Class 5 Peak Conducted Emissions
150kHz to 108MHz



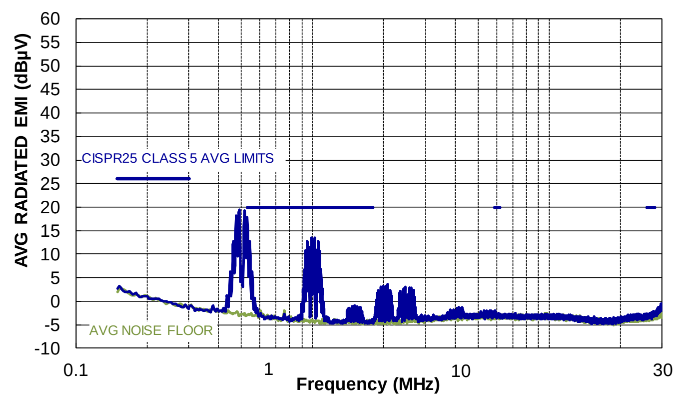
CISPR25 Class 5 Average Conducted Emissions
150kHz to 108MHz



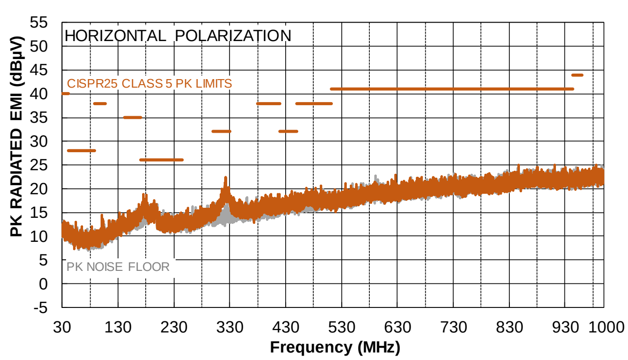
CISPR25 Class 5 Peak Radiated Emissions
150kHz to 30MHz



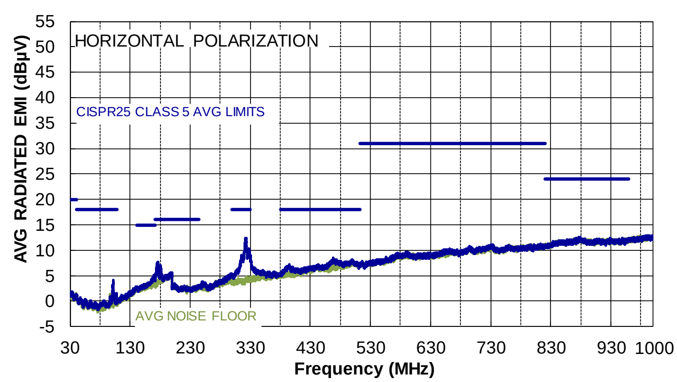
CISPR25 Class 5 Average Radiated Emissions
150kHz to 30MHz



CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz to 1GHz

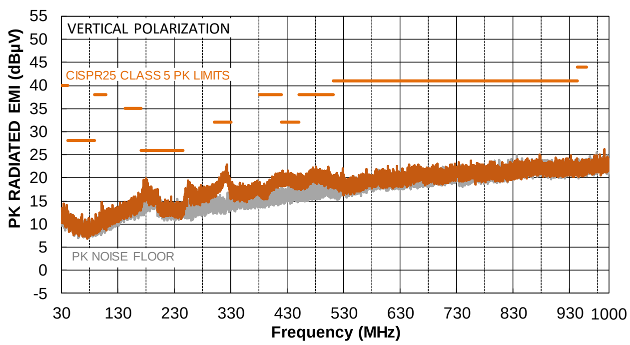


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6μH, C_{OUT} = 94μF, f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted. (8)

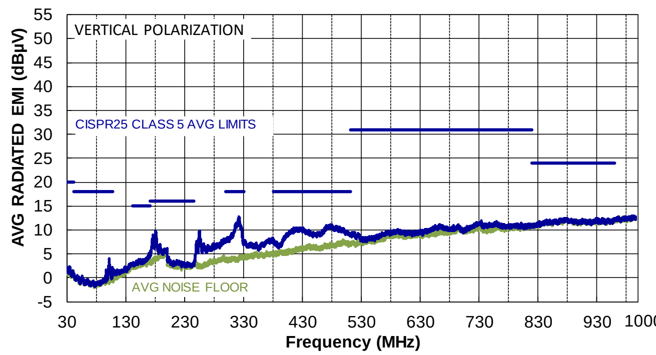
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



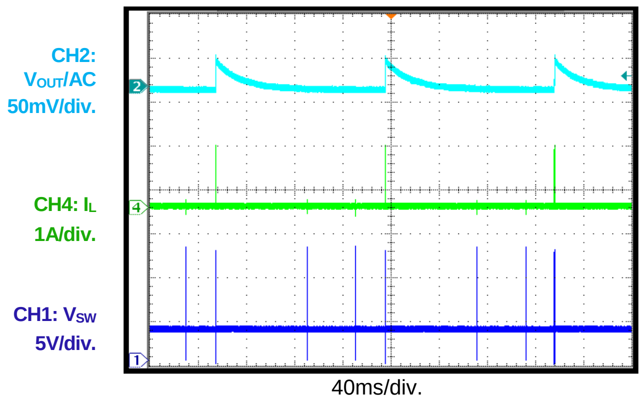
Note:

8) The EMC test results are based on the application circuit with EMI filters (see Figure 13).

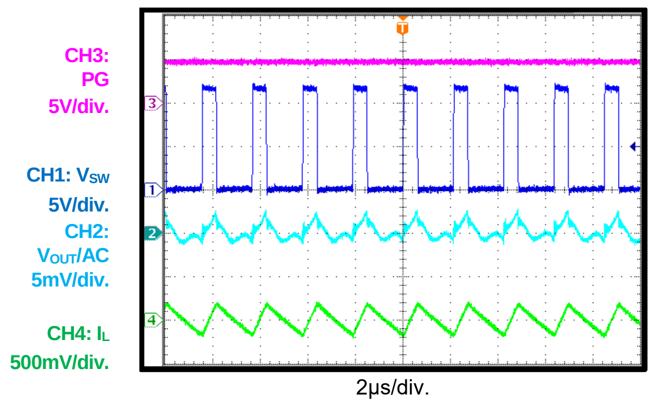
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6μH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

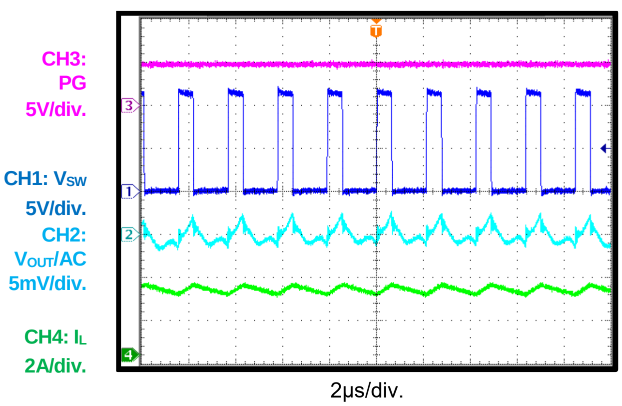
Steady State
I_{OUT} = 0A, AAM



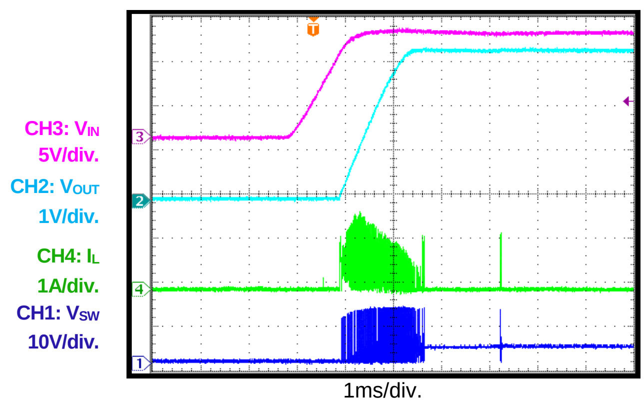
Steady State
I_{OUT} = 0A, FCCM



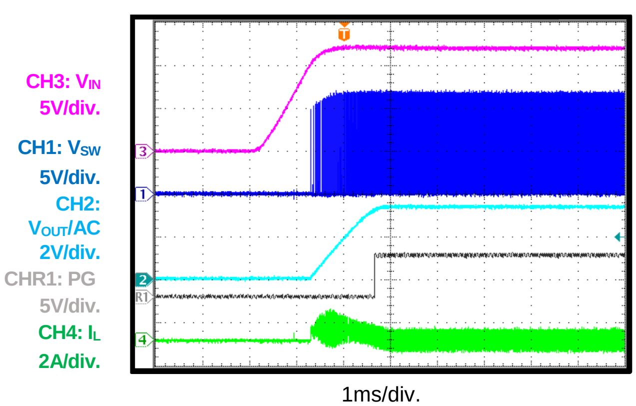
Steady State
I_{OUT} = 3A



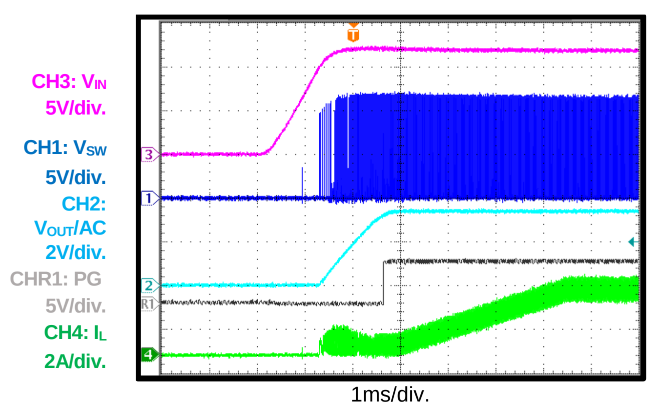
Start-up through VIN
I_{OUT} = 0A, AAM



Start-Up through VIN
I_{OUT} = 0A, FCCM



Start-Up through VIN
I_{OUT} = 3A

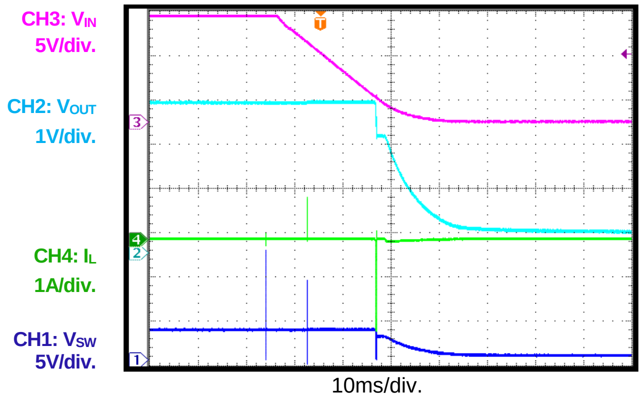


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

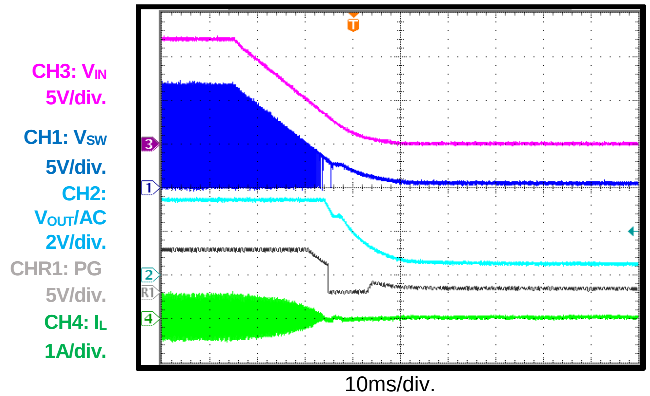
Shutdown through V_{IN}

I_{OUT} = 0A, AAM



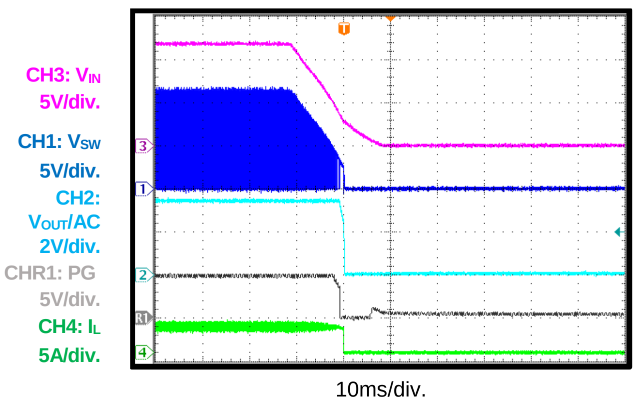
Shutdown through V_{IN}

I_{OUT} = 0A, FCCM



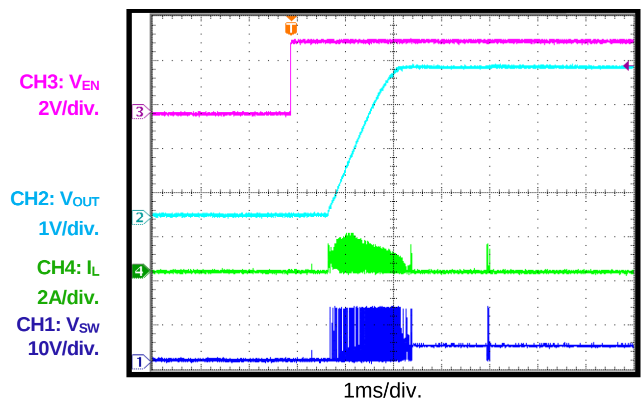
Shutdown through V_{IN}

I_{OUT} = 3A



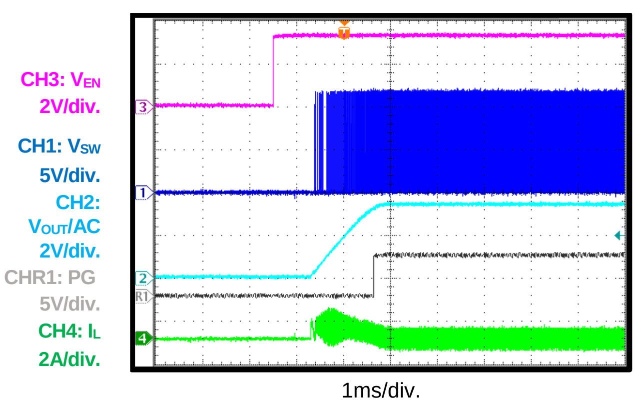
Start-Up through EN

I_{OUT} = 0A, AAM



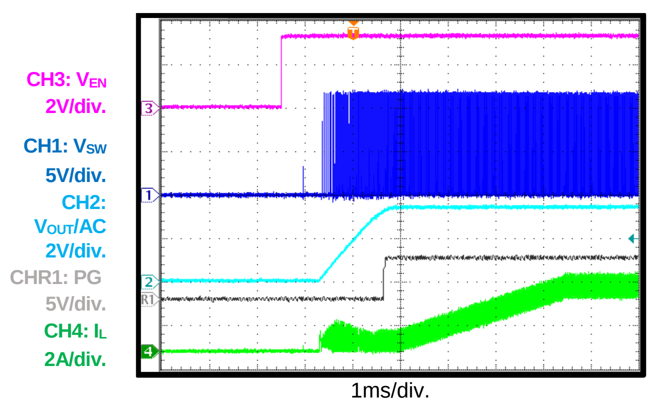
Start-Up through EN

I_{OUT} = 0A, FCCM



Start-Up through EN

I_{OUT} = 3A

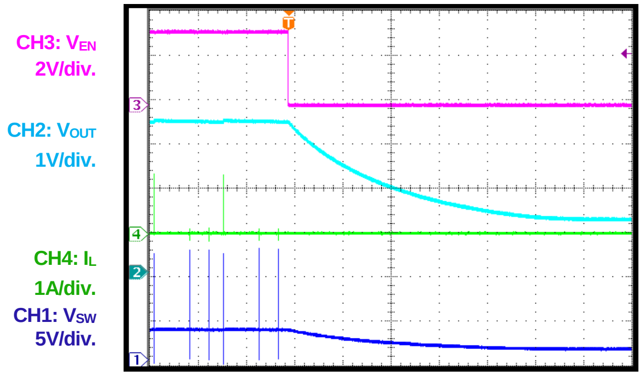


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

Shutdown through EN

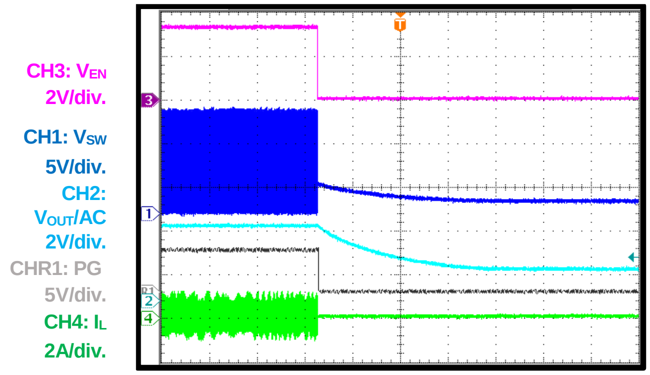
I_{OUT} = 0A, AAM



100ms/div.

Shutdown through EN

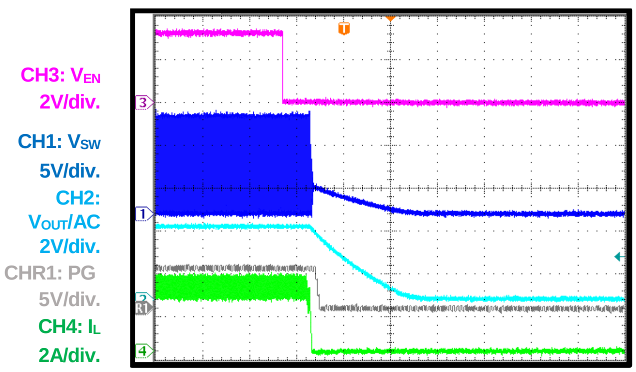
I_{OUT} = 0A, FCCM



100ms/div.

Shutdown through EN

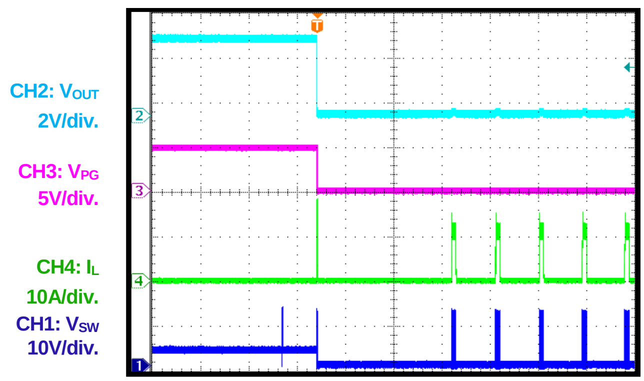
I_{OUT} = 3A



100µs/div.

SCP Entry

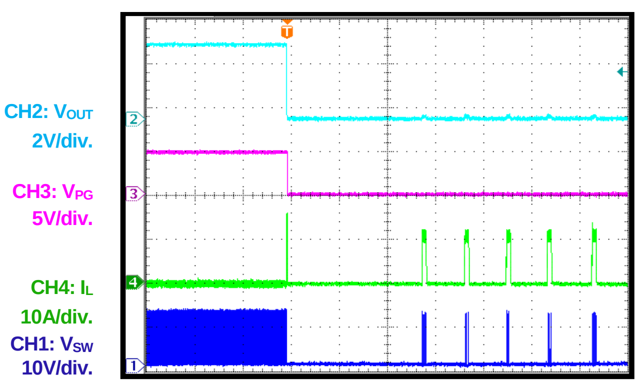
I_{OUT} = 0A, AAM



20ms/div.

SCP Entry

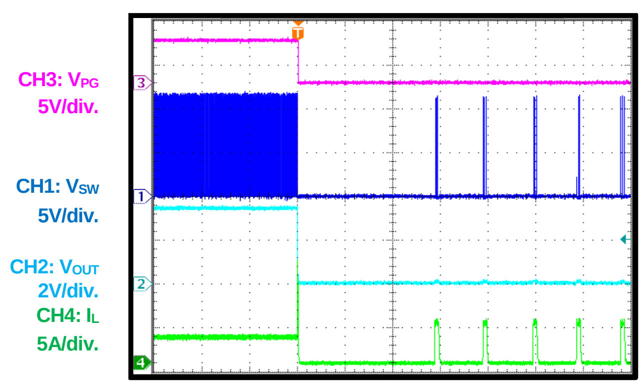
I_{OUT} = 0A, FCCM



20ms/div.

SCP Entry

I_{OUT} = 3A



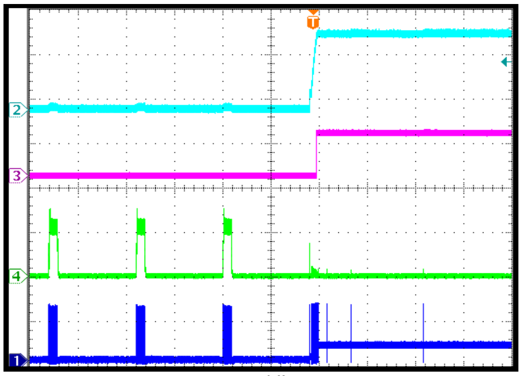
20ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

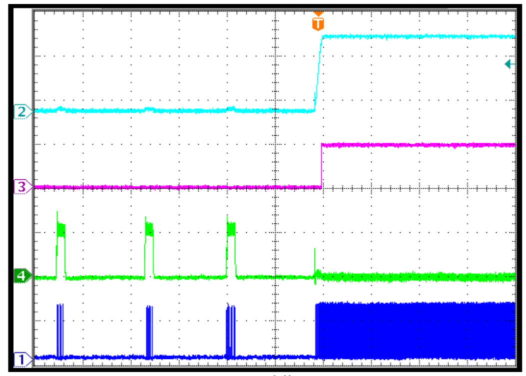
SCP Recovery

I_{OUT} = 0A, AAM



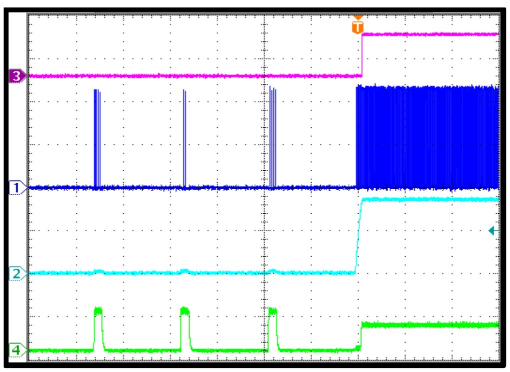
SCP Recovery

I_{OUT} = 0A, FCCM

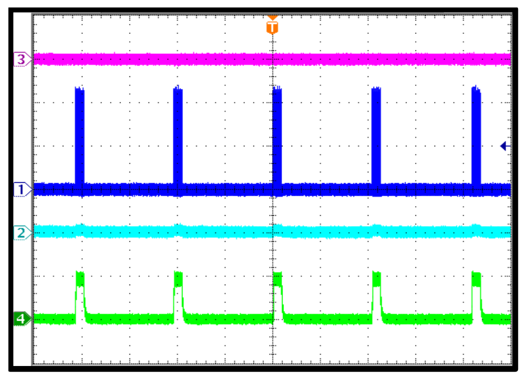


SCP Recovery

I_{OUT} = 3A

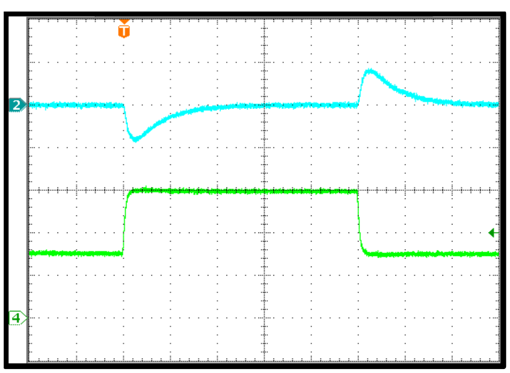


SCP Steady State



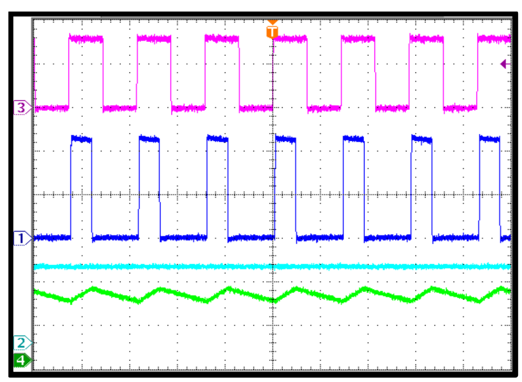
Load Transient

I_{OUT} = 1.5A to 3A, 1.6A/µs



SYNCIN Operation

I_{OUT} = 3A, SYNC frequency = 350kHz

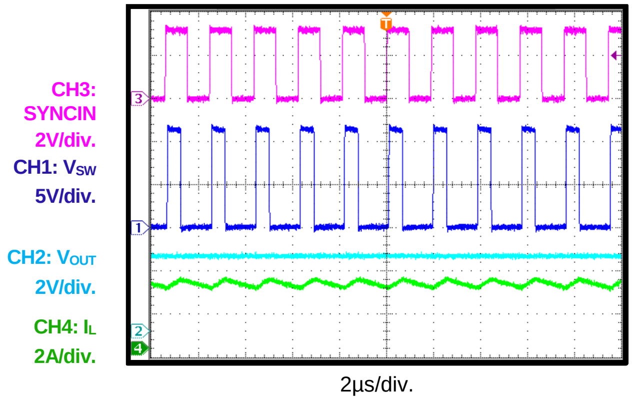


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

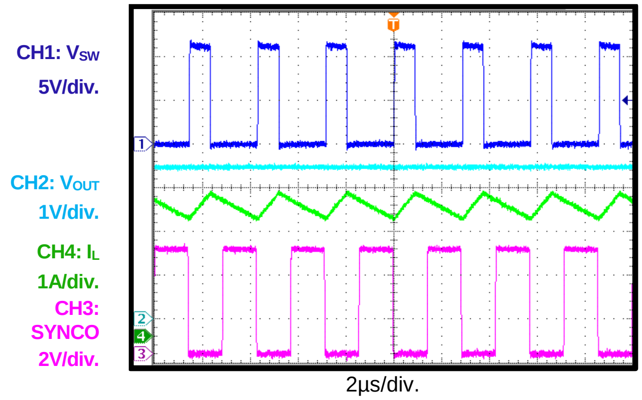
SYNCIN Operation

I_{OUT} = 3A, SYNC frequency = 530kHz



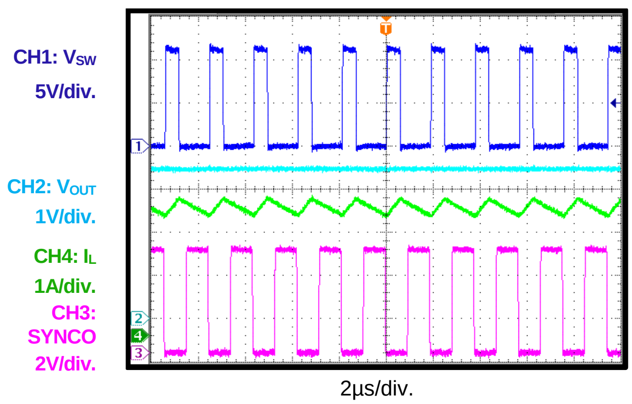
SYNCO Operation

I_{OUT} = 3A, SYNC frequency = 350kHz



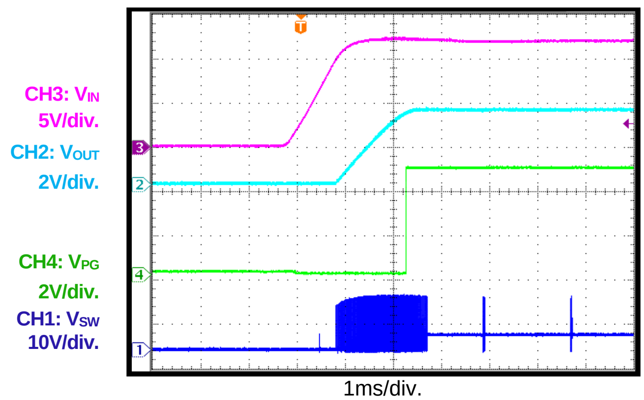
SYNCO Operation

I_{OUT} = 3A, SYNC frequency = 530kHz



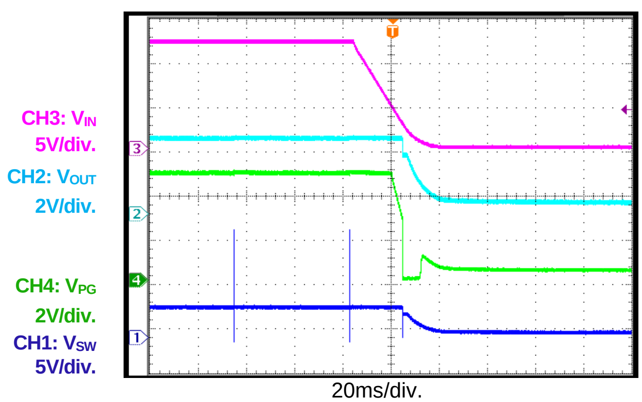
PG in Start-Up through VIN

I_{OUT} = 0A, AAM



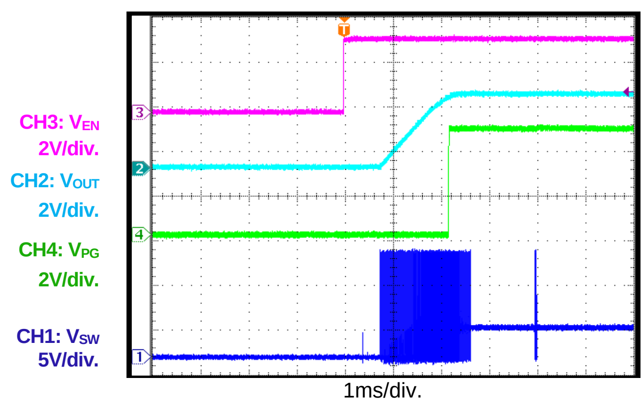
PG in Shutdown through VIN

I_{OUT} = 0A, AAM



PG in Start-Up through EN

I_{OUT} = 0A, AAM

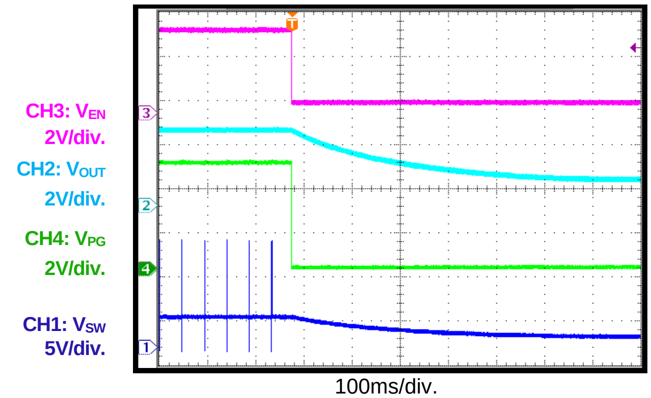


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

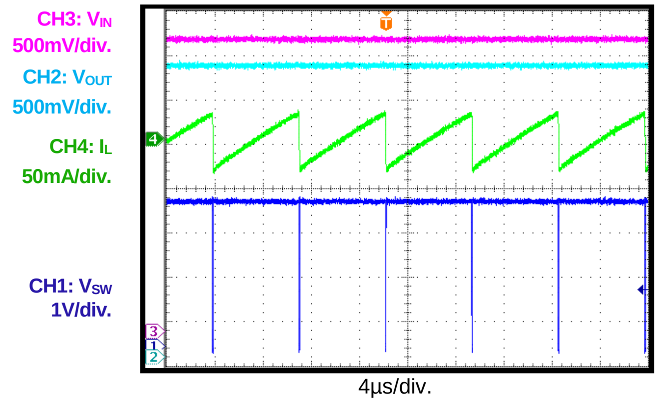
PG in Shutdown through EN

I_{OUT} = 0A, AAM



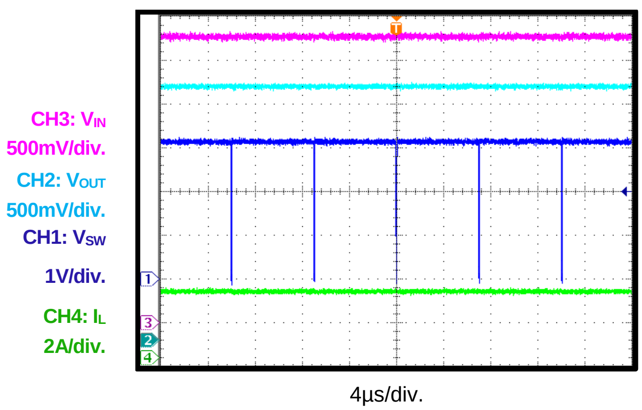
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



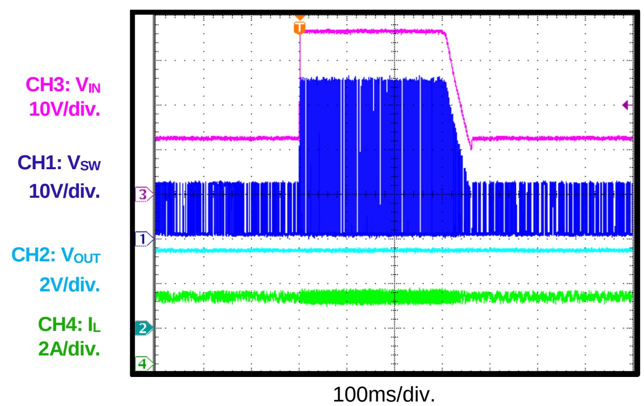
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 3A



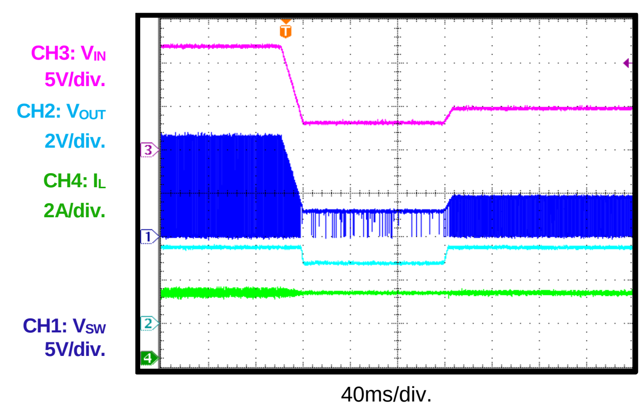
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 3A



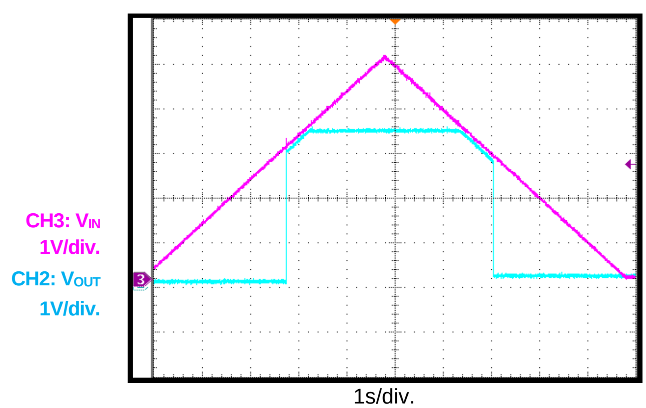
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 3A



VIN Ramp Up and Down

I_{OUT} = 0.1A

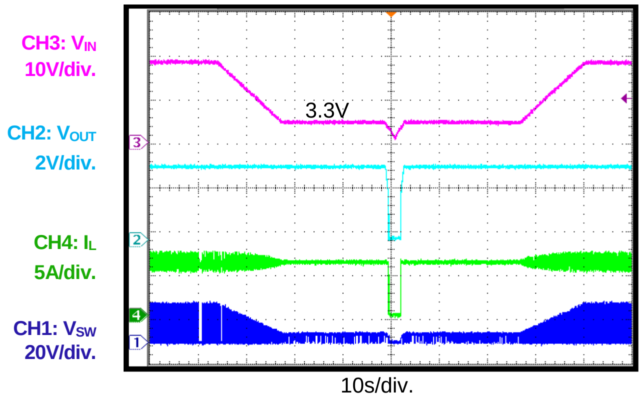


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 5.6µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

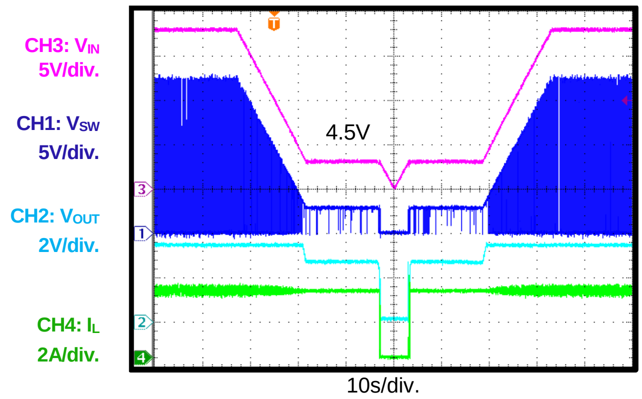
VIN Ramp Down and Up

I_{OUT} = 1mA



VIN Ramp Down and Up

I_{OUT} = 3A



FUNCTIONAL BLOCK DIAGRAM

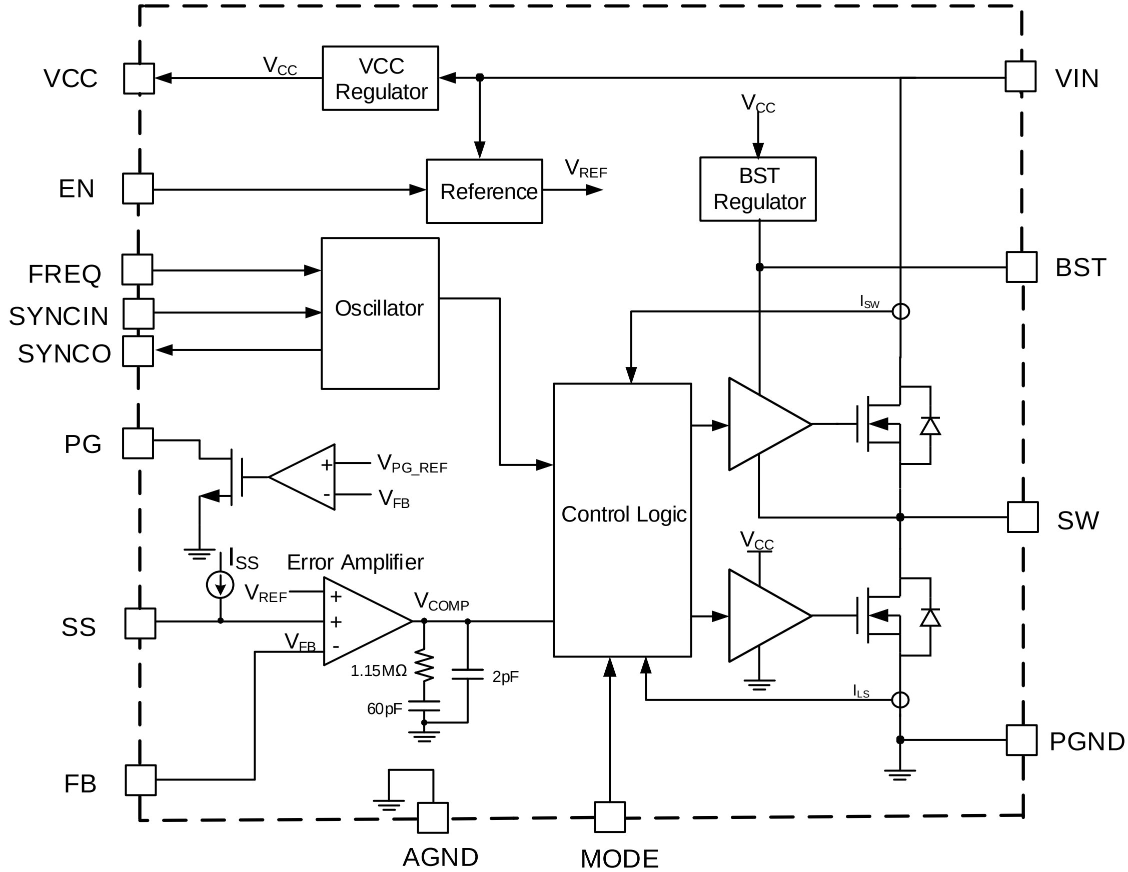


Figure 1: Functional Block Diagram of Adjustable Output Version

FUNCTIONAL BLOCK DIAGRAM *(continued)*

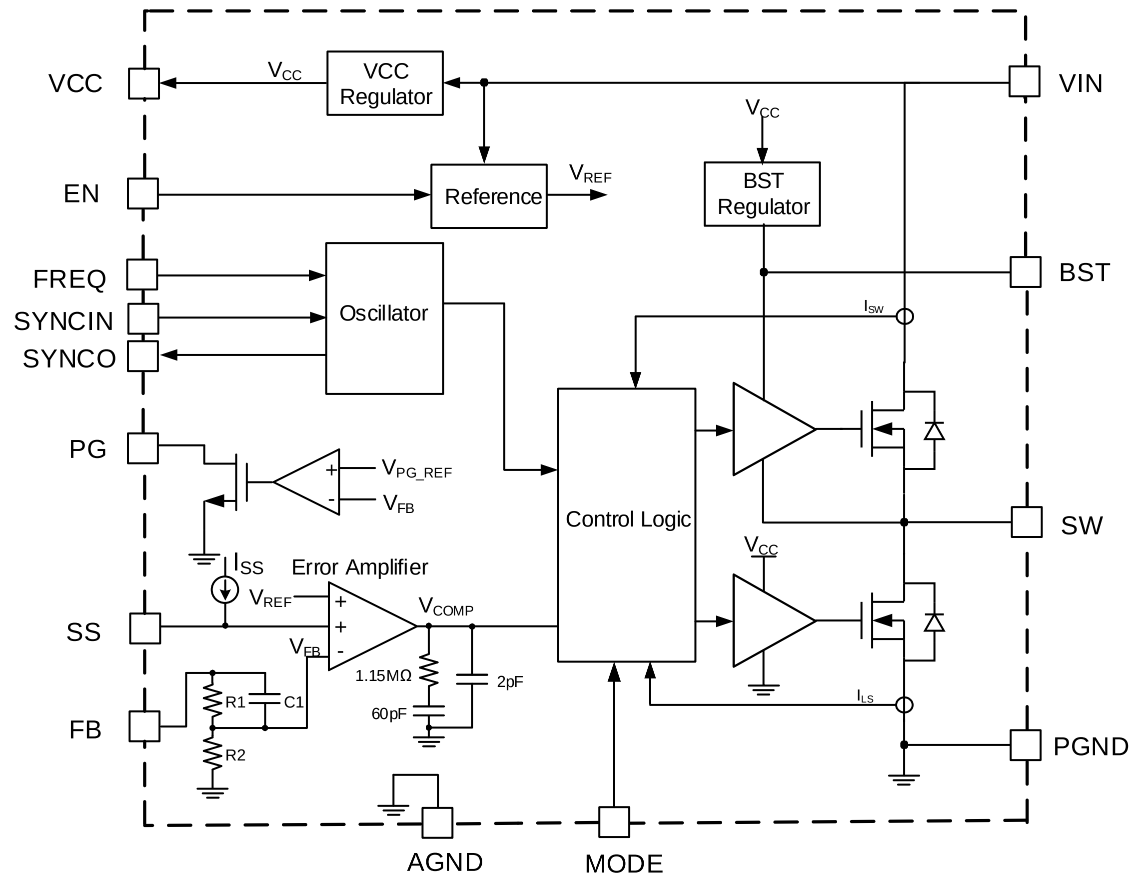


Figure 2: Functional Block Diagram of Fixed Output Version

Timing Sequence Diagram

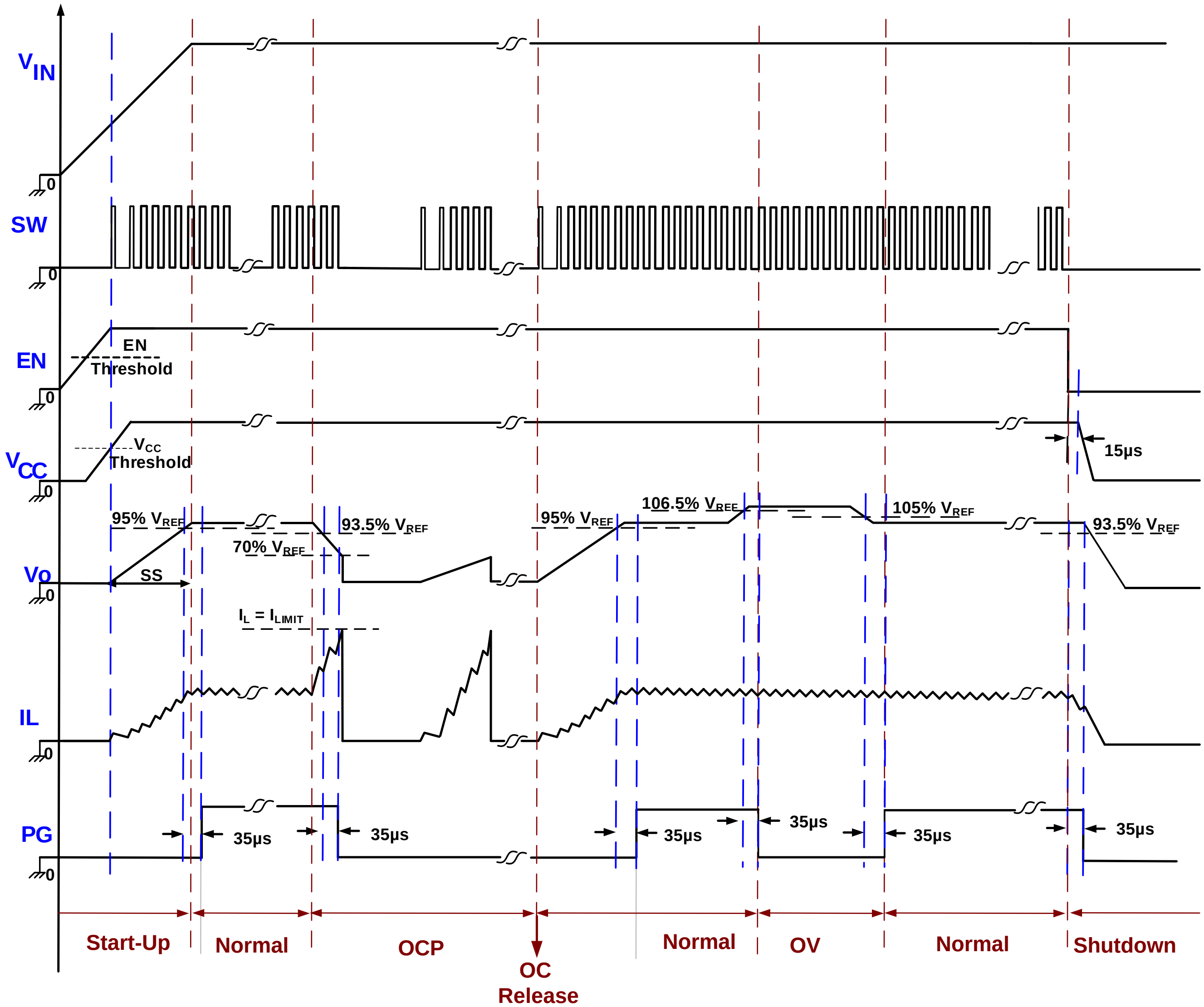


Figure 3: Timing Sequence Diagram

OPERATION

The MPQ4313 is a synchronous, step-down switching regulator with integrated, internal high-side and low-side power MOSFETs. It provides 3A of highly efficient output with current mode control.

It features a wide input voltage range, programmable switching frequency, external soft start, and precision current limiting. The device's very low operational quiescent current makes it suitable for battery-powered applications.

PWM Control

At moderate to high output currents, the MPQ4313 operates in fixed-frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the internal COMP voltage (V_{COMP}). Once the HS-FET is on, it remains on for at least 100ns.

When the HS-FET is off, the low-side MOSFET (LS-FET) turns on immediately and remains on until the next cycle starts. Once the LS-FET is on, it remains on for at least 80ns before the next cycle starts.

If the current in the HS-FET does not reach the COMP set current value within one PWM period, the HS-FET remains on, saving a turn-off operation. The HS-FET is forced off if the on time lasts about 10µs and V_{COMP} is not reached.

Light-Load Operation

In light-load conditions, the MPQ4313 can work in one of two different operation modes by setting the MODE pin to a different status (see Figure 4).

The MPQ4313 works in forced CCM (FCCM) when the CCM pin is pulled above 1.8V. In this mode, the device works with a fixed frequency from no-load to full-load. The advantage of FCCM is the controllable frequency and lower output ripple at light-load.

The MPQ4313 works in asynchronous advanced mode (AAM) when the MODE pin is pulled below 0.4V. AAM optimizes efficiency during light-load and no-load conditions.

When AAM is enabled, the MPQ4313 first enters nonsynchronous operation as long as the inductor current approaches zero at light-load. If the load is further decreased or there is no load that makes the internal COMP voltage (V_{COMP}) decrease to the set value, the MPQ4313 enters AAM. In AAM, the internal clock is reset every time V_{COMP} crosses the set threshold, and the crossover time is taken as the benchmark of the next clock. When the load increases and V_{COMP} exceeds the set value, the operation mode is DCM or CCM, which has a constant switching frequency.

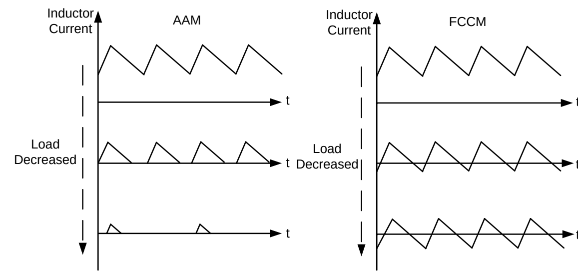


Figure 4: AAM and FCCM

Error Amplifier

The error amplifier compares the FB pin voltage with the internal reference (0.815V) and outputs a current proportional to the difference between the two. This output current is then used to charge the compensation network to form V_{COMP}, which controls the power MOSFET current.

During operation, the minimum V_{COMP} is clamped to 0.9V and its maximum is clamped to 2.0V. In shutdown mode, COMP is pulled down to GND internally.

Internal Regulator VCC

Most of the internal circuitry is powered by the internal 4.9V VCC regulator. This regulator takes V_{IN} as the input and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, VCC is in full regulation. When V_{IN} falls below 4.9V, the output VCC degrades.

Bootstrap Charging

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is below its regulation, a PMOS pass transistor connected from VCC to BST turns on to charge the bootstrap capacitor. External circuitry should provide enough voltage headroom to facilitate charging.

When the HS-FET is on, BST is greater than VCC, so the bootstrap capacitor cannot be charged.

In higher duty cycle operation conditions, the time period available for bootstrap charging is shorter, so the bootstrap capacitor may not charge sufficiently. If the external circuit does not have sufficient voltage and time to charge the bootstrap capacitor, additional external circuitry can be used to ensure the bootstrap voltage is within the normal operation range.

Low-Dropout Mode and BST Refresh

To improve dropout, the MPQ4313 is designed to operate at close to 100% duty cycle as long as the BST-to-SW pin voltage is above 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET is turned off using a UVLO circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor. In DCM mode or PSM mode, the LS-FET is forced on to refresh the BST voltage.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. Thus, the effective duty cycle of the switching regulator is high.

The effective duty cycle during regulator dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode, and the PCB resistance.

Enable Control

EN is a digital control pin that turns the regulator on and off. The MPQ4313 can be enabled in two ways:

First, it can be enabled by an external logic H/L signal. When EN is pulled below the falling threshold voltage (0.85V), the chip is put into the lowest shutdown current mode. Forcing this pin above the EN rising threshold voltage (1V) turns on the part.

The second method is via the programmable VIN under-voltage lockout (UVLO) threshold. With a high enough V_{IN}, the chip can be enabled and disabled by the EN pin. Through the internal current source, this circuit can generate a programmable VIN UVLO and hysteresis (see Figure 5).

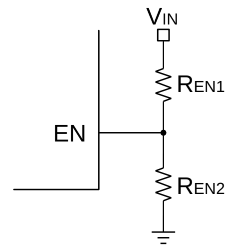


Figure 5: Enable Divider Circuit

Programmable Frequency and Foldback

The MPQ4313 oscillating frequency can be programmed either by an external resistor R_{FREQ} from the FREQ pin to ground, or by a logic-level SYNC signal.

To get a specific switching frequency (f_{SW}), select the R_{FREQ} value following the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics (TPC) section on page 14. Note that f_{SW} will fold back at high V_{IN} when set at high values to avoid triggering the minimum on time and the output going out of regulation. The f_{SW} vs. V_{IN} curve in the TPC section on page 14 shows an example when R_{FREQ} is 12kΩ. The corresponding f_{SW} is about 2.1MHz at V_{IN} = 12V, and falls to less than 1.5MHz when V_{IN} is above 18V. Thus the switching frequency drops into the AM band (<1.8MHz), which should be avoided in car battery applications for EMC compliance. Therefore, the MPQ4313's recommended f_{SW} range for car battery applications is 350kHz to 530kHz. Higher frequencies may still be supported for the applications that do not have critical limits on the switching frequency or have relatively low, stable input voltages.

Frequency Spread Spectrum

The MPQ4313 uses a 12kHz modulation frequency with a 128-step triangular profile to spread the internal oscillator frequency over a 20% (±10%) window. The steps are fixed and independent of the setting oscillator frequency to optimize frequency spread spectrum (FSS) performance.

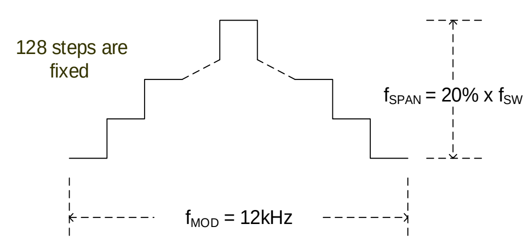


Figure 6: Spread Spectrum Scheme

Side bands are created by modulating the switching frequency with the triangle modulation waveform. The emission power of the fundamental switching frequency and its harmonics is distributed into smaller pieces. This significantly reduces the peak EMI noise.

Soft Start

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up.

When soft start begins, an internal current source begins charging the external soft-start capacitor. Once the soft-start voltage (V_{SS}) is below the internal reference (V_{REF}), V_{SS} overrides V_{REF} and the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, V_{REF} regains control.

The soft-start capacitance (C_{SS}) can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 6.25 \times t_{SS}(ms) \quad (1)$$

The SS pins can be used for tracking and sequencing.

Pre-Biased Start-Up

For the MPQ4313, if $V_{FB} > V_{SS}$ - 150mV at start-up, which means output has a pre-biased voltage, neither the HS-FET nor LS-FET turns on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to prevent thermal runaway. When the silicon die temperature exceeds its upper threshold, it shuts down the power MOSFETs. When the temperature falls below its lower threshold, the chip is enabled again.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current-sense MOSFET. It is then fed to the high-speed current comparator for current mode control. The current comparator takes this sensed current as one of its inputs. When the HS-FET is on, the comparator is blanked until the end of the turn-on transition to avoid noise. Then, the comparator compares the power switch current with the COMP voltage (V_{COMP}). When the sensed current exceeds V_{COMP}, the comparator outputs low to turn off the HS-FET. The maximum current of the internal power MOSFET is internally limited cycle by cycle.

Hiccup Protection

If the output is shorted to ground and the output voltage drops below 70% of its nominal output, the IC shuts down momentarily and begins discharging the soft-start capacitor. It restarts with a full soft start when the soft-start capacitor is fully discharged. This hiccup process repeats until the fault is removed.

Start-Up and Shutdown

If both VIN and EN exceeds their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the MOSFET off for about 50µs to blank any start-up glitches. When the soft-start block is enabled, it keeps the SS output low to ensure the remaining circuitries are ready, then slowly ramps up.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. In the event of a shutdown, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good Output

The MPQ4313 includes an open-drain power good (PG) output that indicates the output. A pull-up resistor to the power source is required if PG is used. The PG output goes high if the output voltage is within 95% to 105% of the nominal voltage, and it goes low if the output voltage is above 106.5% or below 93.5% of the nominal voltage.

SYNCIN and SYNCO

The switching frequency can be synced to the rising edge of the clock signal applied at SYNCIN. The recommended SYNCIN frequency range is 350kHz to 530kHz. Ensure that the off time of SYNCIN is shorter than the period of the internal oscillator, otherwise the internal clock may turn on the HS-FET before the rising edge of SYNCIIN. There is no other specific limit on the pulse width of SYNCIN, but there is always parasitic capacitance of the pad there; so if the pulse width is too short, a clear rising and falling edge may not be seen. A pulse longer than 100ns is recommended in application.

When applying SYNCIN in AAM, drive SYNCIN below its specified threshold (0.4V) or leave SYNCIN floating before the MPQ4313 starts up in AAM. Then add the external SYNCIN clock.

The SYNCO pin provides a default 180° phase-shifted clock to an internal oscillator when there is no SYNCIN signal or a clock signal reverse to SYNCIN if an external clock signal is applied at SYNCIN. This enables easy dual-phase, interleaved configuration.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 8).

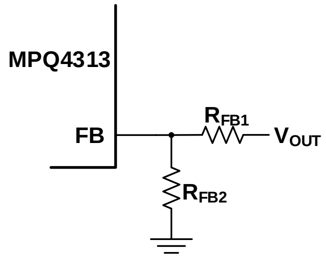


Figure 8: Feedback Network

Calculate R_{FB2} with Equation (2):

$$R_{FB2}=\frac{R_{FB1}}{\frac{V_{OUT}}{0.815V}-1} \quad (2)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	100 (1%)	32.4 (1%)
5	100 (1%)	19.6 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use two 4.7µF to 10µF capacitors. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{CIN}=I_{LOAD}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = $2V_{OUT}$, calculated with Equation (4):

$$I_{CIN}=\frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN}=\frac{I_{LOAD}}{f_{SW}\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times(1-\frac{V_{OUT}}{V_{IN}})\times(R_{ESR}+\frac{1}{8f_{SW}\times C_{OUT}})$$

(6)

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple.

For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_{SW}{}^{2}\times L\times C_{OUT}}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency.

For simplification, the output ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4313 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance.

A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can then be calculated with Equation (9):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (10):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

VIN UVLO Setting

The MPQ4313 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3V, while the falling threshold is about 2.65V. For the applications that need a higher UVLO point, an external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 9).

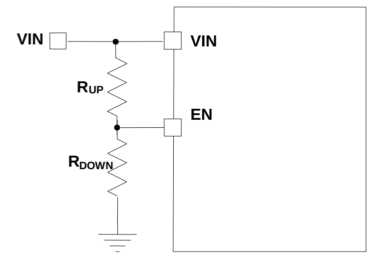


Figure 9: Adjustable UVLO Using EN Divider

The UVLO threshold can be calculated with Equation (11) and Equation (12):

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (11)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (12)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

External BST Diode and Resistor

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external bootstrap diode. VCC or V_{OUT} is recommended to be this power supply in the circuit (see Figure 10).

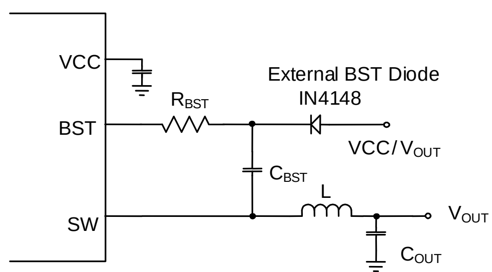


Figure 10: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitance is 0.1µF to 1µF. A resistor in series with the BST capacitor (R_{BST}) can reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at a high V_{IN}. A higher resistance is better for SW spike reduction but compromises efficiency. To make a tradeoff between EMI and efficiency, a ≤20Ω R_{BST} is recommended.

Setting the VCC Capacitor

The VCC capacitor should be 10 times greater than the boost capacitor. A VCC capacitor with a nominal value above 68µF is not recommended.

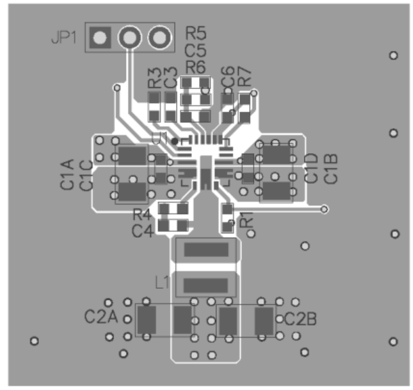
PCB Layout Guidelines [9]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 11 and follow the guidelines below:

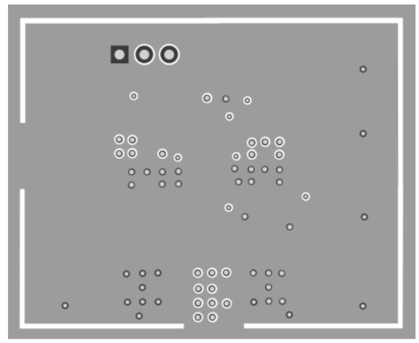
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close as possible to VCC and GND.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

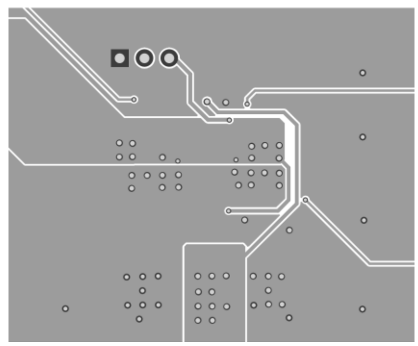
9) The recommended PCB layout is based on Figure 12.



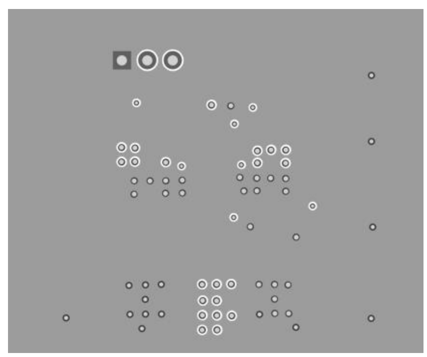
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

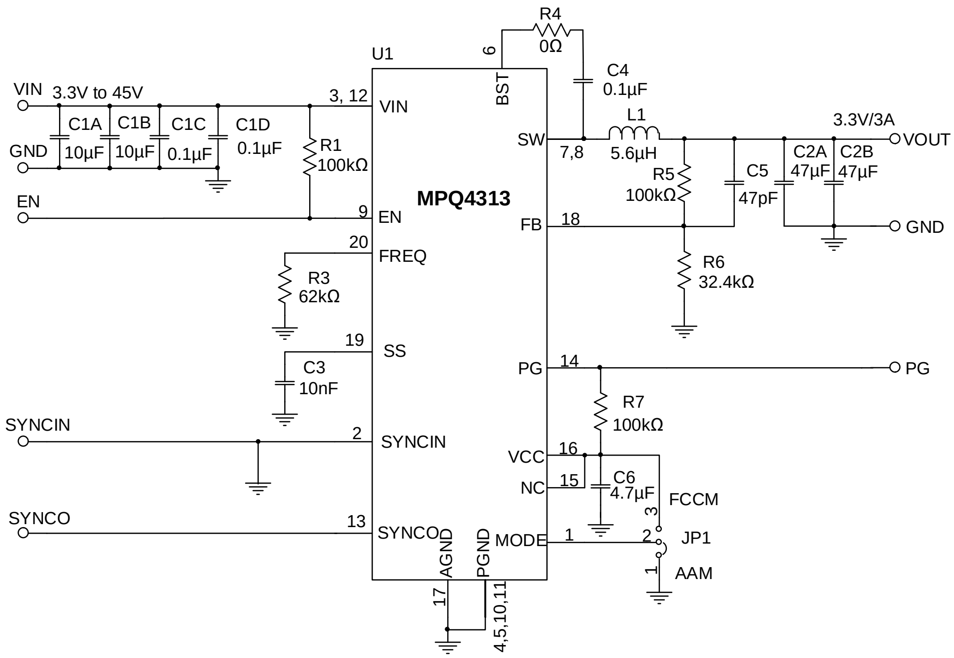


Figure 12: V_{OUT} = 3.3V, f_{SW} = 470kHz

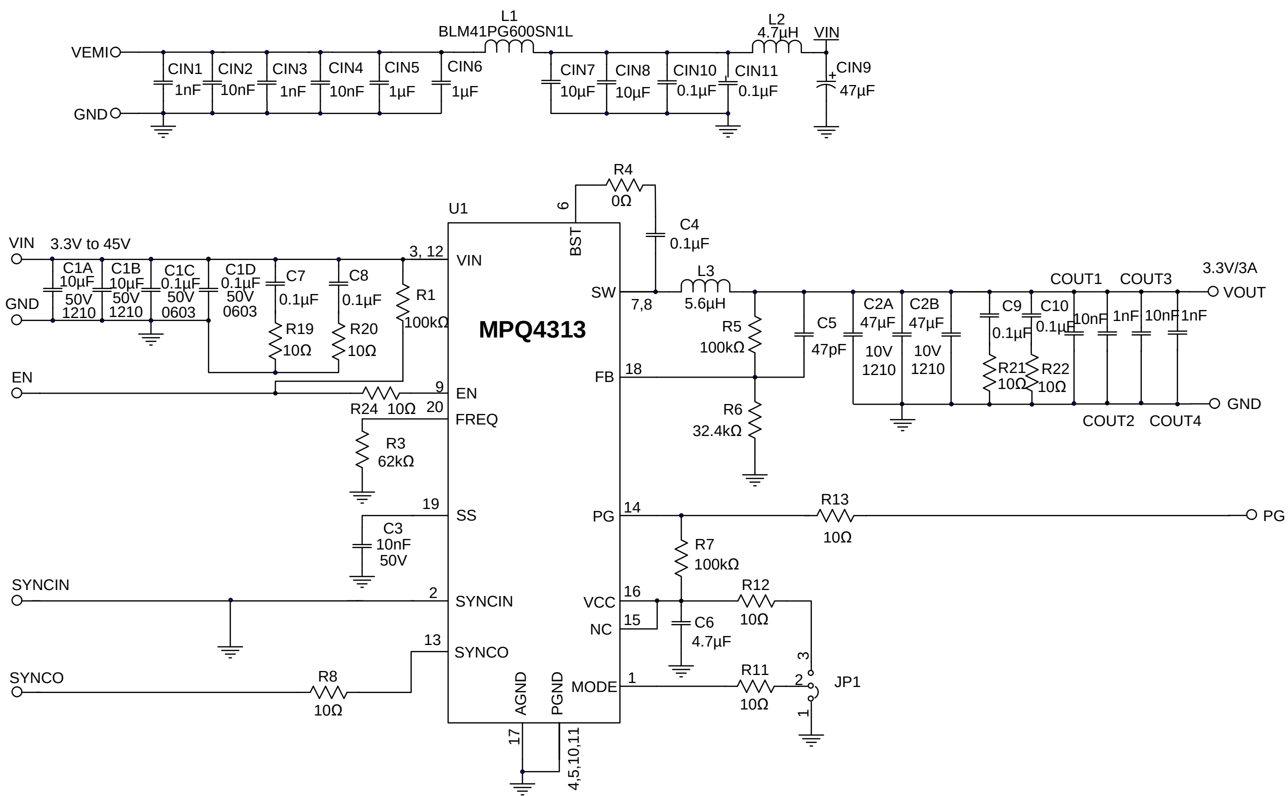


Figure 13: V_{OUT} = 3.3V, f_{SW} = 470kHz with EMI Filters

TYPICAL APPLICATION CIRCUITS *(continued)*

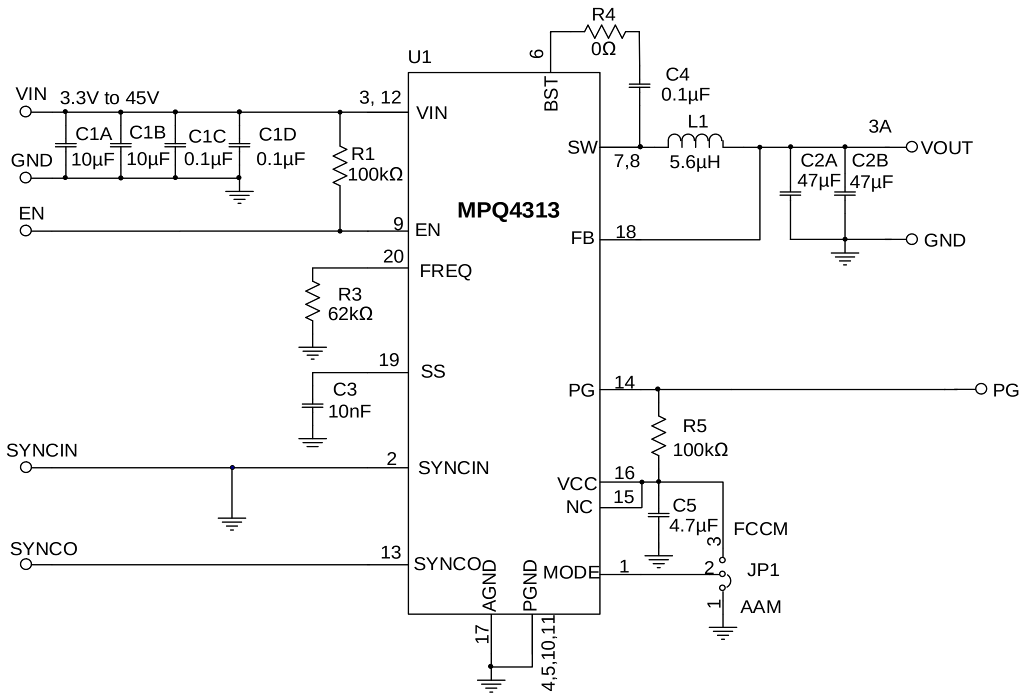
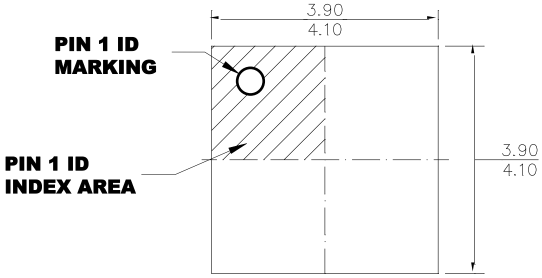


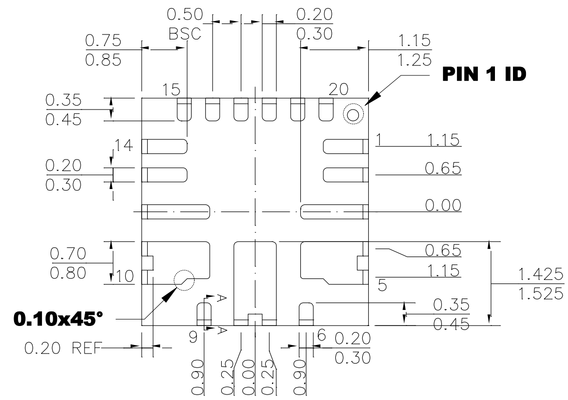
Figure 14: f_{SW} = 470kHz, Fixed Output

PACKAGE INFORMATION

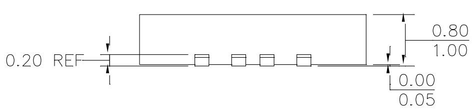
QFN-20 (4mmx4mm)
Wettable Flank



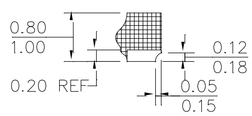
TOP VIEW



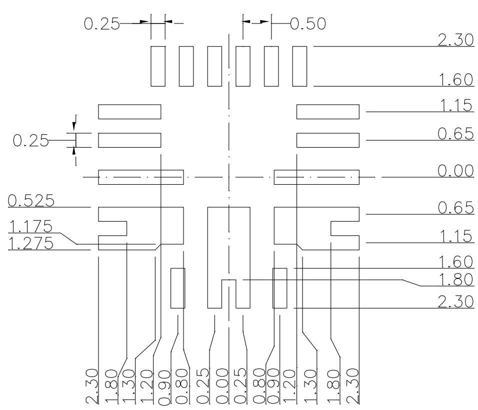
BOTTOM VIEW



SIDE VIEW



SECTION A-A

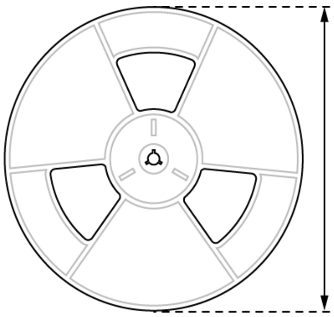


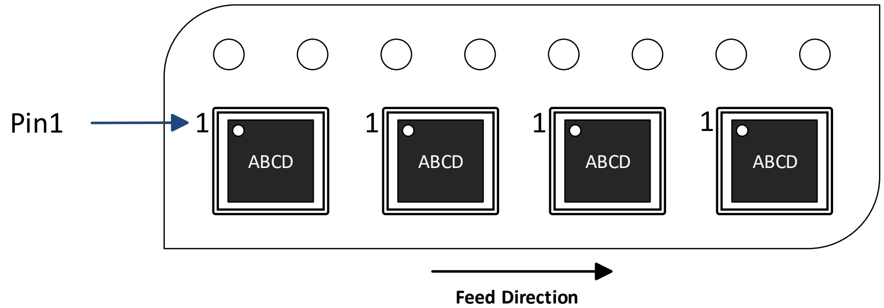
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity /Reel	Quantity /Tube (10)	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4313GRE-AEC1–Z MPQ4313GRE-33-AEC1–Z MPQ4313GRE-5-AEC1–Z	QFN-20 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

10) N/A indicates "not available" in tubes. For 500-piece tape & reel prototype quantities, contact the factory. (Order code for 500-piece partial reel is "–P", tape & reel dimensions remain the same as the full reel.)

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	6/5/2020	Initial Release	-