

## Features

- Low Offset Voltage: 10  $\mu$ V (Max)
- Zero Drift: 0.008  $\mu$ V/ $^{\circ}$ C
- 0.1-Hz to 10-Hz Noise: 1.1  $\mu$ V<sub>PP</sub>
- Low Supply Current: 42  $\mu$ A per Amplifier
- Bandwidth: 350 kHz
- Slew Rate: 0.16 V/ $\mu$ s
- High-Gain, 130-dB High CMRR and PSRR
- Rail-to-Rail Input and Output Swing
- Operating Temperature Range:  $-40^{\circ}$ C to  $125^{\circ}$ C
- Small Packages: SOT353 (SC70-5) and SOT23-5 (TP5531)

## Applications

- Transducer Amplifier
- Bidirectional Current Sense
- DC Offset Correction
- Temperature Measurement
- Remote Located Sensors
- Battery-Powered Instruments
- Electronic Weigh Scales

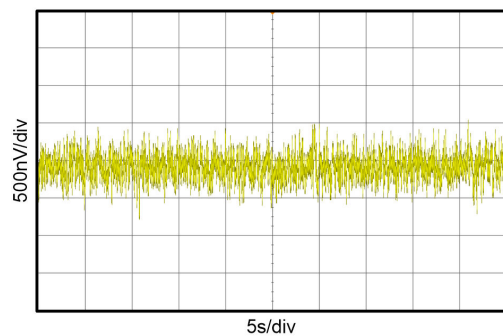
## Description

The 3PEAK TP5531/5532/5534 is a series of low-power chopper-stabilized operational amplifiers that provide input offset voltage correction for low offset and offset drift over time and temperature. The series operates with a single supply voltage as low as 1.8 V, while drawing a quiescent current of 42  $\mu$ A per amplifier with a gain bandwidth product of 350 kHz. The series is unity-gain stable, and has no 1/f noise. It also has a good power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR), and features the rail-to-rail input and output swing.

The series is designed using an advanced CMOS process. The TP5531 (single version) is available in the SOT353 (SC70-5), SOT23-5, and SOP8 packages. The TP5532 (dual version) is offered in the MSOP8 and SOP8 packages. The TP5534 (quad version) is available in the TSSOP14 and SOP14 packages. All versions are specified for operation from  $-40^{\circ}$ C to  $125^{\circ}$ C.

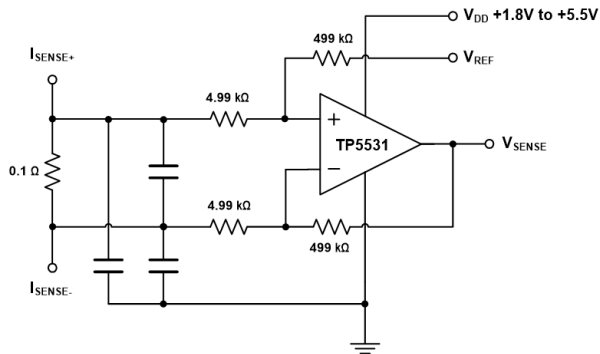
### Related Zero-Drift Op Amps

V <sub>OS</sub> (Max)	10 $\mu$ V	5 $\mu$ V
GBWP	350 kHz	3.5 MHz
Supply Current	42 $\mu$ A	500 $\mu$ A
e <sub>N</sub> at 1 kHz	55 nV/ $\sqrt$ Hz	15 nV/ $\sqrt$ Hz
Single	TP5531	TP5551
Dual	TP5532	TP5552
Quad	TP5534	TP5554

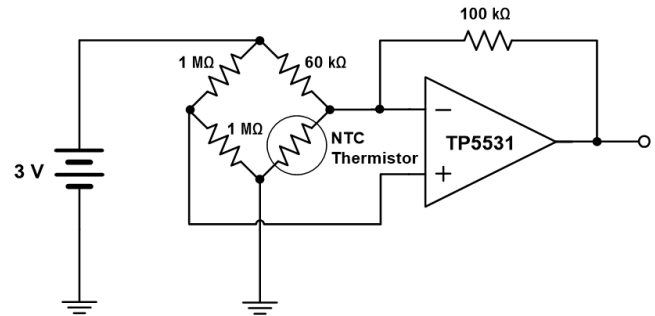


**0.1-Hz to 10-Hz Noise**

## Typical Application Circuit



**Bi-Directional Current Sense Amplifier**



**Thermistor Measurement**

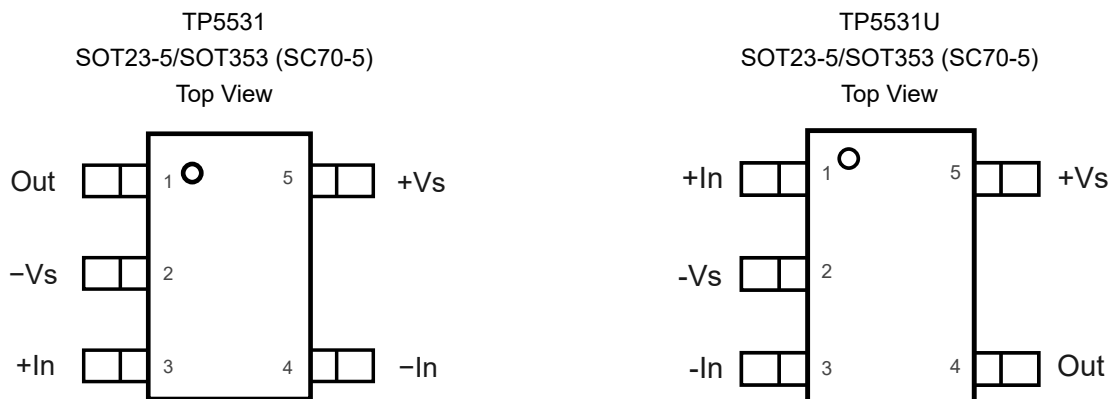
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## Revision History

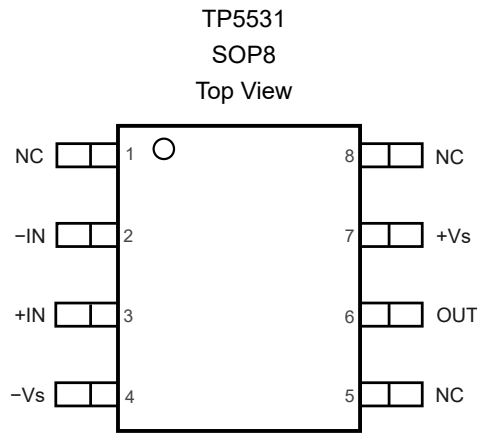
Date	Revision	Notes
	Rev.B.1	Updated the Package Outline Dimensions of DFN2X2-8. Deleted the part numbers which are not in manufacturing: TP5531-CR, TP5531-SR.
2025-01-04	Rev.B.2	Added the Tape and Reel Information. The following updates are all about the new datasheet formats or typo, the actual product remains unchanged. Updated to a new datasheet format. Updated the Package Outline Dimensions.

## Pin Configuration and Functions

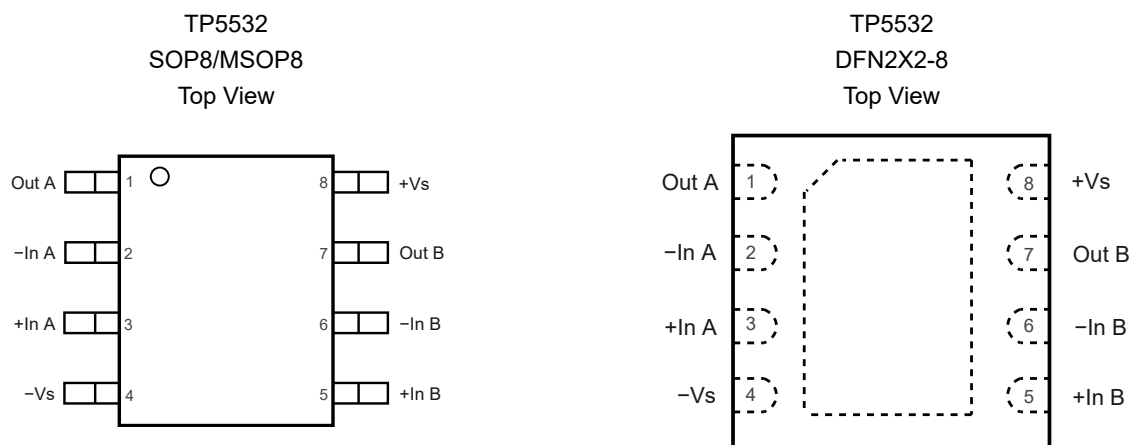


**Table 1. Pin Functions: TP5531, TP5531U**

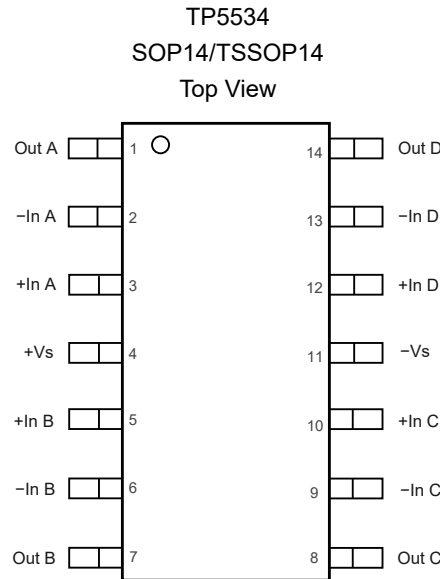
Pin No.		Name	I/O	Description
TP5531	TP5531U			
1	4	Out	O	Output of the amplifier. The voltage range extends to within millivolts of each supply rail.
2	2	$-V_S$	Power Supply	Negative power supply. It is normally tied to GND. It can also be tied to a voltage other than GND when the voltage between $+V_S$ and $-V_S$ is from 1.8 V to 5.5 V. If it is not connected to GND, bypass it with a capacitor of 0.1 $\mu$ F to the part as close as possible.
3	1	+In	I	Non-inverting input of the amplifier.
4	3	-In	I	Inverting input of the amplifier.
5	5	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 1.8 V to 5.5 V. Split supplies are possible when the voltage between $+V_S$ and $-V_S$ is between 1.8 V and 5.5 V. A bypass capacitor of 0.1 $\mu$ F to the part as close as possible should be used between the power supply pins or between supply pins and GND.

**1.8-V, 42- $\mu$ A, RRIO, Zero-Drift Operational Amplifier**

**Table 2. Pin Functions: TP5531**

Pin No.	Name	I/O	Description
1	NC		Not connected.
2	-IN	I	Inverting input of the amplifier.
3	+IN	I	Non-inverting input of the amplifier.
4	-V <sub>S</sub>	Power Supply	Negative power supply. It is normally tied to GND. It can also be tied to a voltage other than GND when the voltage between +V <sub>S</sub> and -V <sub>S</sub> is from 1.8 V to 5.5 V. If it is not connected to GND, bypass it with a capacitor of 0.1 $\mu$ F to the part as close as possible.
5	NC		Not connected.
6	Out	O	Amplifier output. The voltage range extends to within mV of each supply rail.
7	+V <sub>S</sub>	Power Supply	Positive power supply. Typically, the voltage is from 1.8 V to 5.5 V. Split supplies are possible when the voltage between +V <sub>S</sub> and -V <sub>S</sub> is between 1.8 V and 5.5 V. A bypass capacitor of 0.1 $\mu$ F to the part as close as possible should be used between the power supply pins or between supply pins and ground.
8	NC		Not connected.

**1.8-V, 42- $\mu$ A, RRIO, Zero-Drift Operational Amplifier**

**Table 3. Pin Functions: TP5532**

Pin No.	Name	I/O	Description
1	Out A	O	Output of the amplifier. The voltage range extends to within millivolts of each supply rail.
2	-In A	I	Inverting input of the amplifier.
3	+In A	I	Non-inverting input of the amplifier.
4	-Vs	Power Supply	Negative power supply. It is normally tied to GND. It can also be tied to a voltage other than GND when the voltage between +Vs and -Vs is from 1.8 V to 5.5 V. If it is not connected to GND, bypass it with a capacitor of 0.1 $\mu$ F to the part as close as possible.
5	+In B	I	Non-inverting input of the amplifier.
6	-In B	I	Inverting input of the amplifier.
7	Out B	O	Output of the amplifier. The voltage range extends to within millivolts of each supply rail.
8	+Vs	Power Supply	Positive power supply. Typically, the voltage is from 1.8 V to 5.5 V. Split supplies are possible when the voltage between +Vs and -Vs is between 1.8 V and 5.5 V. A bypass capacitor of 0.1 $\mu$ F to the part as close as possible should be used between the power supply pins or between supply pins and GND.
	Thermal Pad		The thermal pad of the DFN2X2-8 package is recommended to be floating or connected to -Vs.

**1.8-V, 42- $\mu$ A, RRIO, Zero-Drift Operational Amplifier**

**Table 4. Pin Functions: TP5534**

Pin No.	Name	I/O	Description
1	Out A	O	Output of the amplifier. The voltage range extends to within millivolts of each supply rail.
2	-In A	I	Inverting input of the amplifier.
3	+In A	I	Non-inverting input of the amplifier.
4	+Vs	Power Supply	Positive power supply. Typically, the voltage is from 1.8 V to 5.5 V. Split supplies are possible when the voltage between +Vs and -Vs is between 1.8 V and 5.5 V. A bypass capacitor of 0.1 $\mu$ F to the part as close as possible should be used between the power supply pins or between supply pins and GND.
5	+In B	I	Non-inverting input of the amplifier.
6	-In B	I	Inverting input of the amplifier.
7	Out B	O	Output of the amplifier. The voltage range extends to within millivolts of each supply rail.
8	Out C	O	Output of the amplifier. The voltage range extends to within millivolts of each supply rail.
9	-In C	I	Inverting input of the amplifier.
10	+In C	I	Non-inverting input of the amplifier.
11	-Vs	Power Supply	Negative power supply. It is normally tied to GND. It can also be tied to a voltage other than GND when the voltage between +Vs and -Vs is from 1.8 V to 5.5 V. If it is not connected to GND, bypass it with a capacitor of 0.1 $\mu$ F to the part as close as possible.
12	+In D	I	Non-inverting input of the amplifier.
13	-In D	I	Inverting input of the amplifier.
14	Out D	O	Output of the amplifier. The voltage range extends to within millivolts of each supply rail.



## Specifications

### Absolute Maximum Ratings <sup>(1)</sup>

Parameter		Min	Max	Unit
	Supply Voltage		6	V
	Input Voltage	$(-V_S) - 0.2$	$(+V_S) + 0.2$	V
	Input Current: +IN, -IN <sup>(2)</sup>	-20	20	mA
	Output Short-Circuit Duration <sup>(3)</sup>		Indefinite	
	Current at Supply Pins	-50	50	mA
T <sub>J</sub>	Maximum Junction Temperature		150	°C
T <sub>A</sub>	Operating Temperature Range	-40	125	°C
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C
T <sub>L</sub>	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.

(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. The thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

### ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### Thermal Information

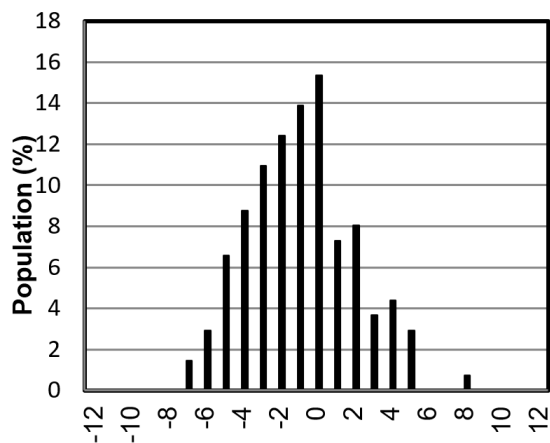
Package Type	θ <sub>JA</sub>	θ <sub>JC</sub>	Unit
SOT353 (SC70-5)	250		°C/W
SOT23-5	200		°C/W
MSOP8	210		°C/W
SOP8	158		°C/W
SOP14	83		°C/W
TSSOP14	100		°C/W

## Electrical Characteristics

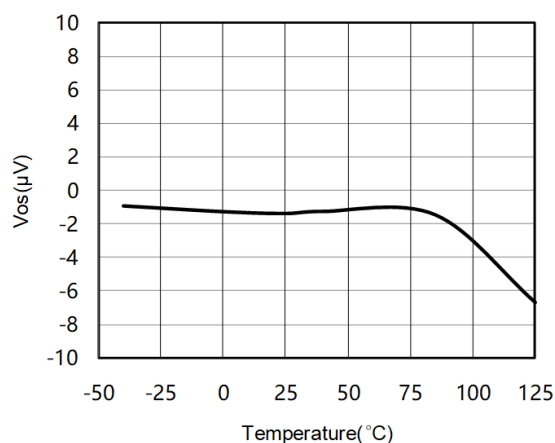
All test conditions:  $V_S = 5\text{ V}$ ,  $T_A = 27^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{CM} = V_{DD} / 2$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_S$	Supply Voltage Range		1.8		5.5	V
$I_Q$	Quiescent Current per Amplifier	TP5531		45	65	$\mu\text{A}$
		TP5532/TP5534		42	60	$\mu\text{A}$
$V_{OS}$	Input Offset Voltage	$V_{CM} = 2.5\text{ V}$	-10	1	10	$\mu\text{V}$
		$V_{CM} = 0.05\text{ V to } 4.95\text{ V}$	-20		20	$\mu\text{V}$
		$V_S = 1.8\text{ V}$ , $V_{CM} = 0.9\text{ V}$	-20		20	$\mu\text{V}$
$dV_{OS}/dT$	$V_S$ Power Supply			0.008	0.05	$\mu\text{V}/^\circ\text{C}$
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{ V to } 5\text{ V}$	100	120		dB
$V_n$	Input Voltage Noise	$f = 0.01\text{ Hz to } 1\text{ Hz}$		0.4		$\mu\text{V}_{PP}$
		$f = 0.1\text{ Hz to } 10\text{ Hz}$		1.1		$\mu\text{V}_{PP}$
$e_n$	Input Voltage Noise Density	$f = 1\text{ kHz}$		55		$\text{nV}/\sqrt{\text{Hz}}$
$C_{IN}$	Input Capacitor	Differential mode		3		pF
		Common mode		2		pF
$I_B$	Input Bias Current			$\pm 50$		pA
	Over Temperature			$\pm 800$		pA
$I_{OS}$	Input Offset Current			$\pm 100$		pA
$V_{CM}$	Common-Mode Voltage Range		$(-V_S) - 0.1$		$(+V_S) + 0.1$	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0.5\text{ V to } 4.5\text{ V}$	100	120		dB
$V_O$	Output Voltage Swing from Rail	$R_L = 10\text{ k}\Omega$		10	25	mV
$I_{SC}$	Short-Circuit Current			$\pm 60$		mA
GBWP	Unity Gain Bandwidth	$C_L = 100\text{ pF}$		350		kHz
SR	Slew Rate	$G = +1$ , $C_L = 100\text{ pF}$		0.16		$\text{V}/\mu\text{s}$
$t_{OR}$	Overload Recovery Time	$G = -10$		60		$\mu\text{s}$
$t_s$	Settling Time, 0.01%	$C_L = 100\text{ pF}$ , $G = +1$ , 5-V step		40		$\mu\text{s}$
$A_{VOL}$	Open-Loop Voltage Gain	$(-V_S) + 100\text{ mV} < V_O < (+V_S) - 100\text{ mV}$ , $R_L = 100\text{ k}\Omega$	100	120		dB

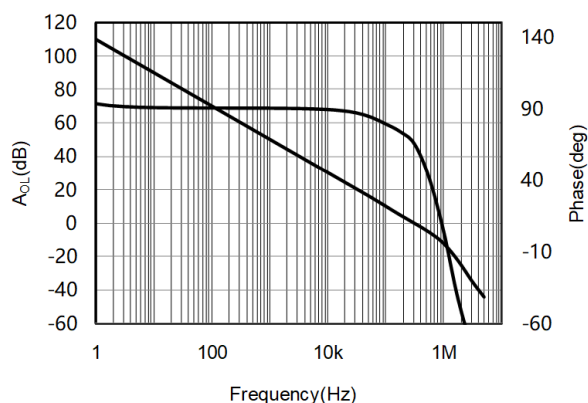
## Typical Performance Characteristics



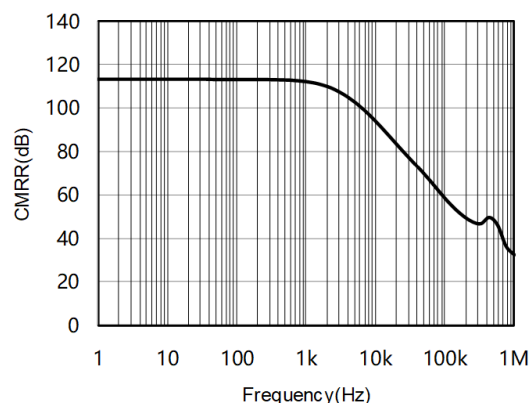
**Figure 1. Offset Voltage Distribution**



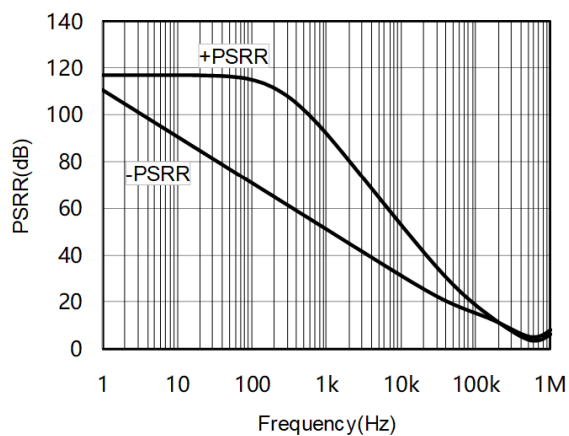
**Figure 2. Offset Voltage vs. Temperature**



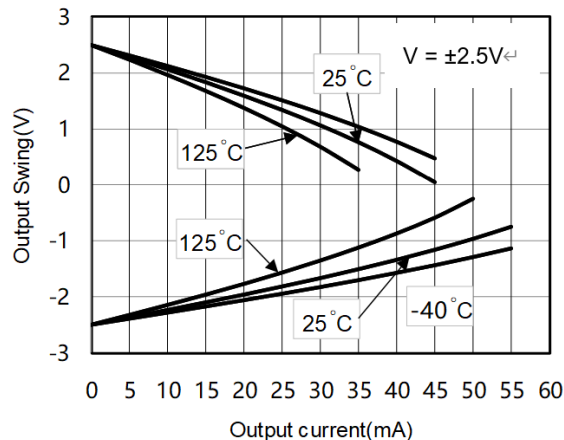
**Figure 3. Open-Loop Gain vs. Frequency**



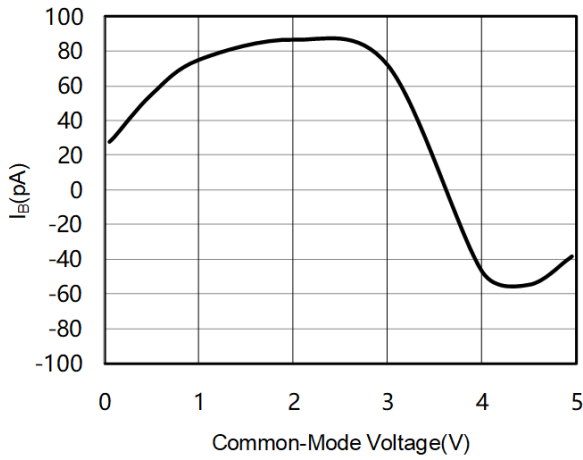
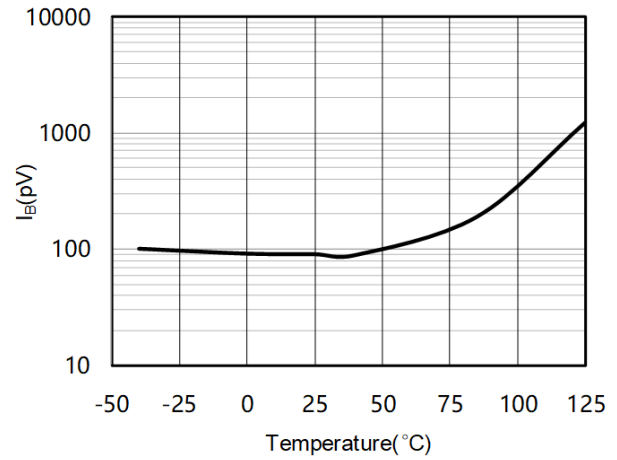
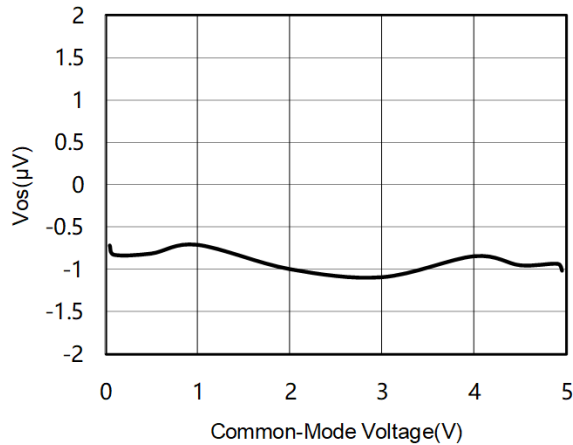
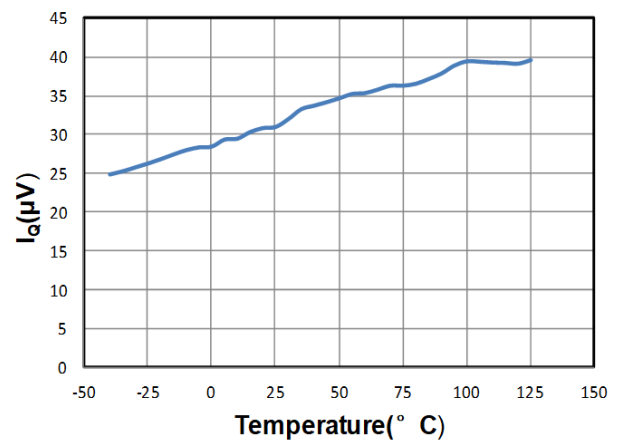
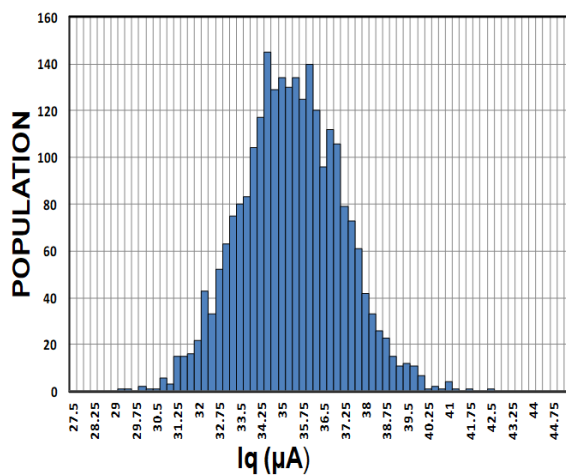
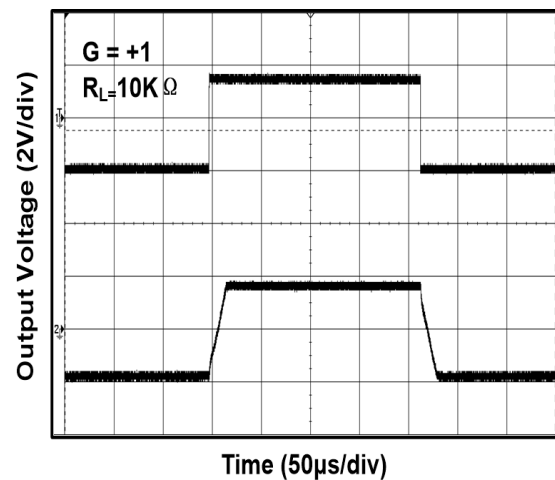
**Figure 4. CMRR vs. Frequency**

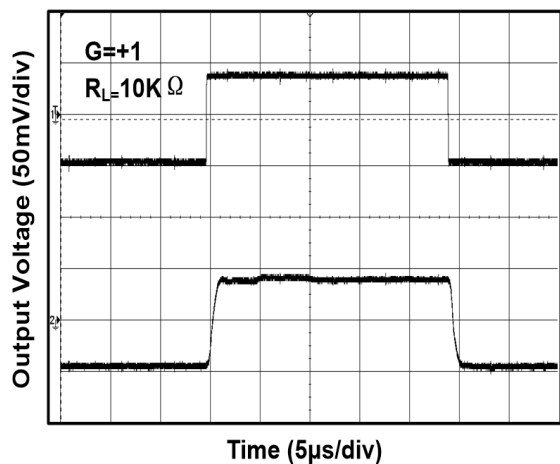
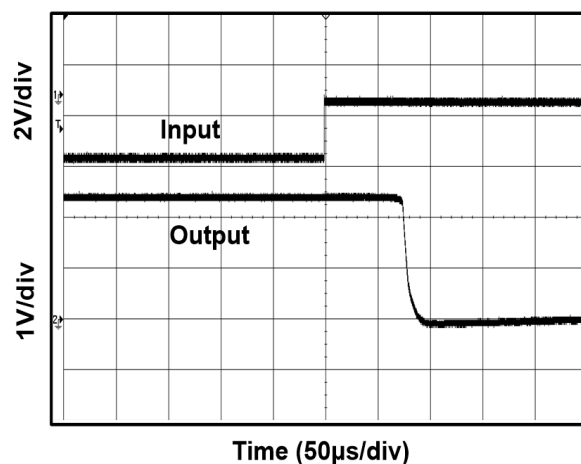
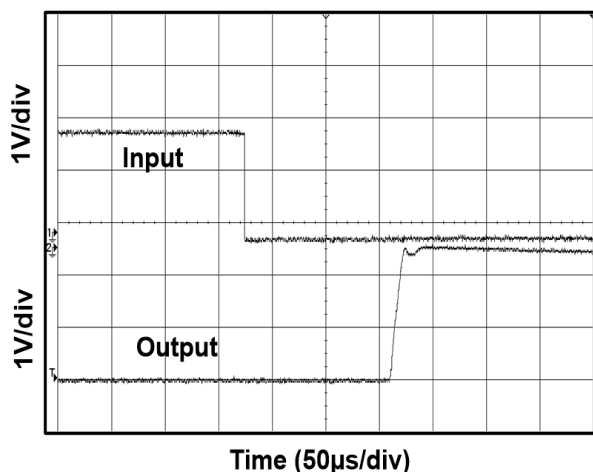
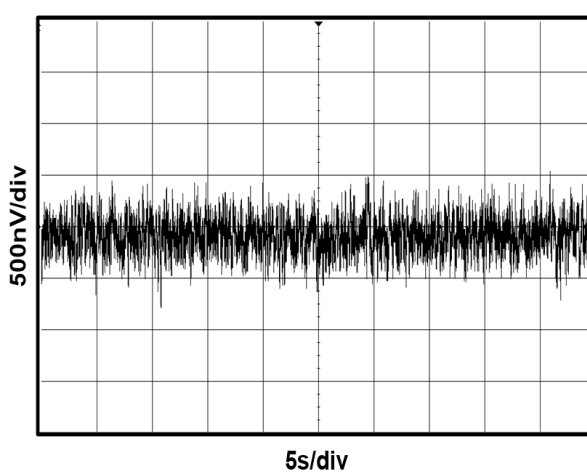
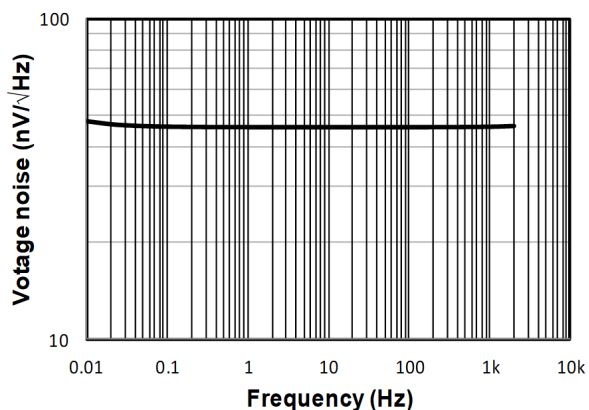


**Figure 5. PSRR vs. Frequency**



**Figure 6. Output Swing vs. Load Current**


**Figure 7.  $I_B$  vs. Common-Mode Voltage**

**Figure 8. Input Bias vs. Temperature**

**Figure 9.  $V_{OS}$  vs. Common-Mode Voltage**

**Figure 10. Quiescent Current vs. Temperature**

**Figure 11. Quiescent Current Distribution**

**Figure 12. Large-Scale Step Response**


**Figure 13. Small-Scale Step Response**

**Figure 14. Positive Over-Voltage Recovery**

**Figure 15. Negative Over-Voltage Recovery**

**Figure 16. 0.1-Hz to 10-Hz Noise**

**Figure 17. Voltage Noise Spectral Density vs. Frequency**

## Detailed Description

### Overview

The TP553x is a series of zero-drift, rail-to-rail operation amplifiers that can be run from a single-supply voltage. The series uses an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path while consuming a supply current of only 42  $\mu$ A per channel. The amplifier is zero-corrected with a 120-kHz clock. Upon power-up, the amplifier requires approximately 100  $\mu$ s to achieve specified  $V_{OS}$  accuracy. This design has no aliasing or flicker noise.

## Application and Implementation

### Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

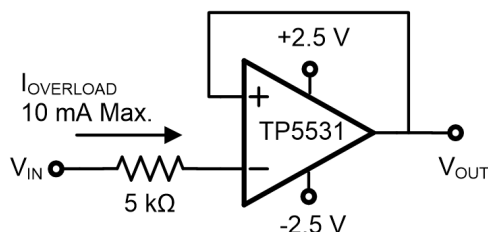
## Application Information

### Rail-to-Rail Input and Output

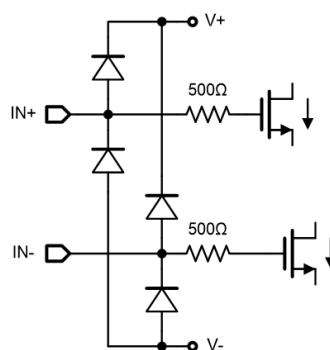
The TP553x series features rail-to-rail inputs and outputs with a supply voltage from 1.8 V to 5.5 V. This allows the inputs of the amplifier to have a wide common-mode range (50 mV beyond supply rails) while maintaining high CMRR (130 dB) and maximizes the signal-to-noise ratio of the amplifier by having the  $V_{OH}$  and  $V_{OL}$  levels at the  $+V_S$  and  $-V_S$  rails, respectively.

### Input Protection

The TP553x series has internal ESD protection diodes that are connected between the inputs and supply rails. When either input exceeds one of the supply rails by more than 300 mV, the ESD diodes become forward-biased, and large amounts of current begin to flow through them. Without current limitation, this excessive fault current causes permanent damage to the device. Thus an external series resistor must be used to ensure that the input currents never exceed 10 mA.



Current-limiting resistor required if input voltage exceeds supply rails by  $>0.5V$ .



INPUT ESD DIODE CURRENT LIMITING-  
UNITY GAIN

Figure 18. Input Protection

### Low Input Referred Noise

The flicker noise, as known as the  $1/f$  noise, is inherent in semiconductor devices, and increases as the frequency decreases. So at lower frequencies, the flicker noise dominates, causing higher degrees of error for sub-Hertz frequencies or DC precision applications.

The TP553x series is a chopper-stabilized amplifier, and the flicker noise is reduced greatly because of this technique. This reduction in the  $1/f$  noise allows the TP553x series to have much lower noise at DC and low frequency compared to standard low-noise amplifiers.

### Residual Voltage Ripple

The chopping technique can be used in the design of the amplifier due to the internal notch filter. Although the chopping-related voltage ripple is suppressed, higher noise spectrum exists at the chopping frequency and its harmonics due to the residual ripple.

So if the frequency of the input signal is near the chopping frequency, the signal may be interfered by the residue ripple. To further suppress the noise at the chopping frequency, it is recommended that a post filter be placed at the output of the amplifier.

### Broad Band and External Resistor Noise Considerations

The total broadband noise output from any amplifier is primarily a function of three types of noise: the input voltage noise from the amplifier, the input current noise from the amplifier, and the thermal (Johnson) noise from the external resistors used around the amplifier. These noise sources are not correlated with each other, and their combined noise can be summed in a root sum squared manner. The full equation is given as:

$$e_{n\text{total}} = \left[ e_n^2 + 4kTR_S + (i_n \times R_S)^2 \right]^{1/2} \quad (1)$$

Where:

$e_n$  = the input voltage noise density of the amplifier;

$i_n$  = the input current noise of the amplifier;

$R_S$  = the source resistance connected to the non-inverting terminal;

$k$  = the Boltzmann's constant ( $1.38 \times 10^{-23}$  J/K).

$T$  = the ambient temperature in Kelvin (K).

The total equivalent RMS noise over a specific bandwidth is expressed as:

$$e_{n,\text{rms}} = e_{n\text{total}} \times \sqrt{BW} \quad (2)$$

The input voltage noise density ( $e_n$ ) of the TP553x series is 55 nV/√Hz, and the input current noise can be neglected. When the source resistance is 190 kΩ, the voltage noise contribution from the source resistor and the amplifier are equal. With a source resistance greater than 190 kΩ, the overall noise of the system is dominated by the Johnson noise of the resistor itself.

### High Source Impedance Application

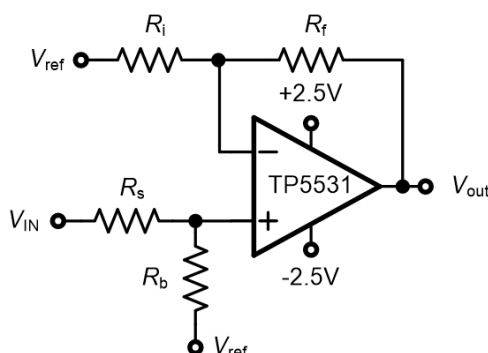
The TP553x series uses switches at the input of the chopper amplifier, and the input signal is chopped at 125 kHz to reduce the input offset voltage down to 10 μV. The dynamic behavior of these switches induces a charge injection current to the input terminals of the amplifier. The charge injection current has a DC path to ground through the resistances seen at the input terminals of the amplifier. Higher input impedance causes an apparent shift in the input bias current of the amplifier.

Because the chopper amplifier has charge injection currents at each terminal, the input offset current is larger than that of standard amplifiers. The  $I_{OS}$  of the TP553x series are 150 pA under the typical condition. So the input impedance should be balanced across each input. The input impedance of the amplifier should be matched between the +IN and -IN terminals to minimize the total input offset current. Input offset currents show up as an additional output offset voltage, as shown in [Equation 3](#).

$$V_{OS,\text{total}} = V_{OS} - R_f \times I_{OS} \quad (3)$$

For a gain configure using a 1-MΩ feedback resistor, a 150-pA total input offset current has an additional output offset voltage of 0.15 mV. By keeping the input impedance low and balanced across the amplifier inputs, the input offset current effect can be suppressed efficiently.



**1.8-V, 42- $\mu$ A, RRIO, Zero-Drift Operational Amplifier**


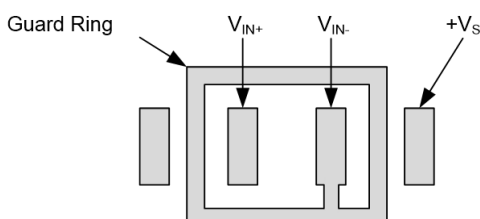
**Figure 19. Circuit Implication for Reducing Input Offset Current Effect**

**PCB Surface Leakage**

In applications where the low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. The surface leakage is caused by humidity, dust, or other contamination on the board. It is recommended to use the multi-layer PCB layout and route the  $-IN$  and  $+IN$  signal of the device under the PCB surface.

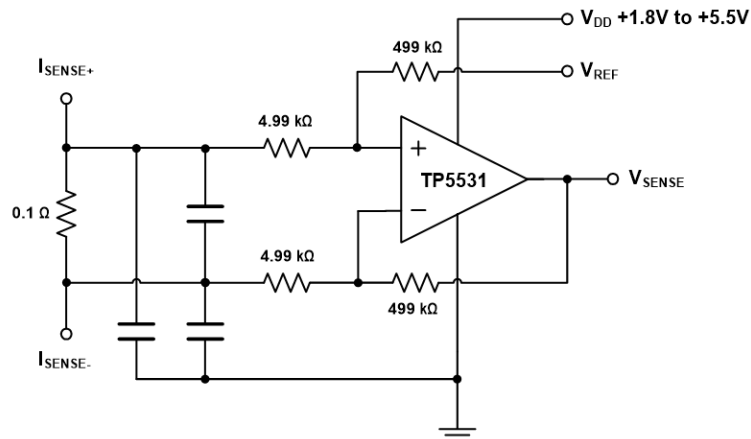
An effective way to reduce surface leakage is to use a guard ring around the sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in [Figure 20](#) for inverting gain applications.

1. For non-inverting gain and unity-gain buffers:
  - a. Connect the non-inverting pin ( $V_{+IN}$ ) to the input with a wire that does not touch the PCB surface.
  - b. Connect the guard ring to the inverting input pin ( $V_{-IN}$ ). This biases the guard ring to the common-mode input voltage.
2. For inverting gain and trans-impedance gain amplifiers (convert current to voltage, such as photo detectors):
  - a. Connect the guard ring to the non-inverting input pin ( $V_{+IN}$ ). This biases the guard ring to the same reference voltage as the operational amplifier (e.g.,  $V_{DD} / 2$  or ground).
  - b. Connect the inverting pin ( $V_{-IN}$ ) to the input with a wire that does not touch the PCB surface.

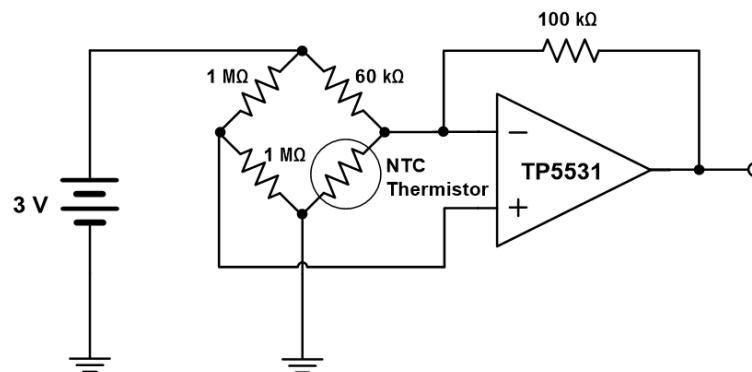


**Figure 20. The Layout of Guard Ring**

## Typical Application

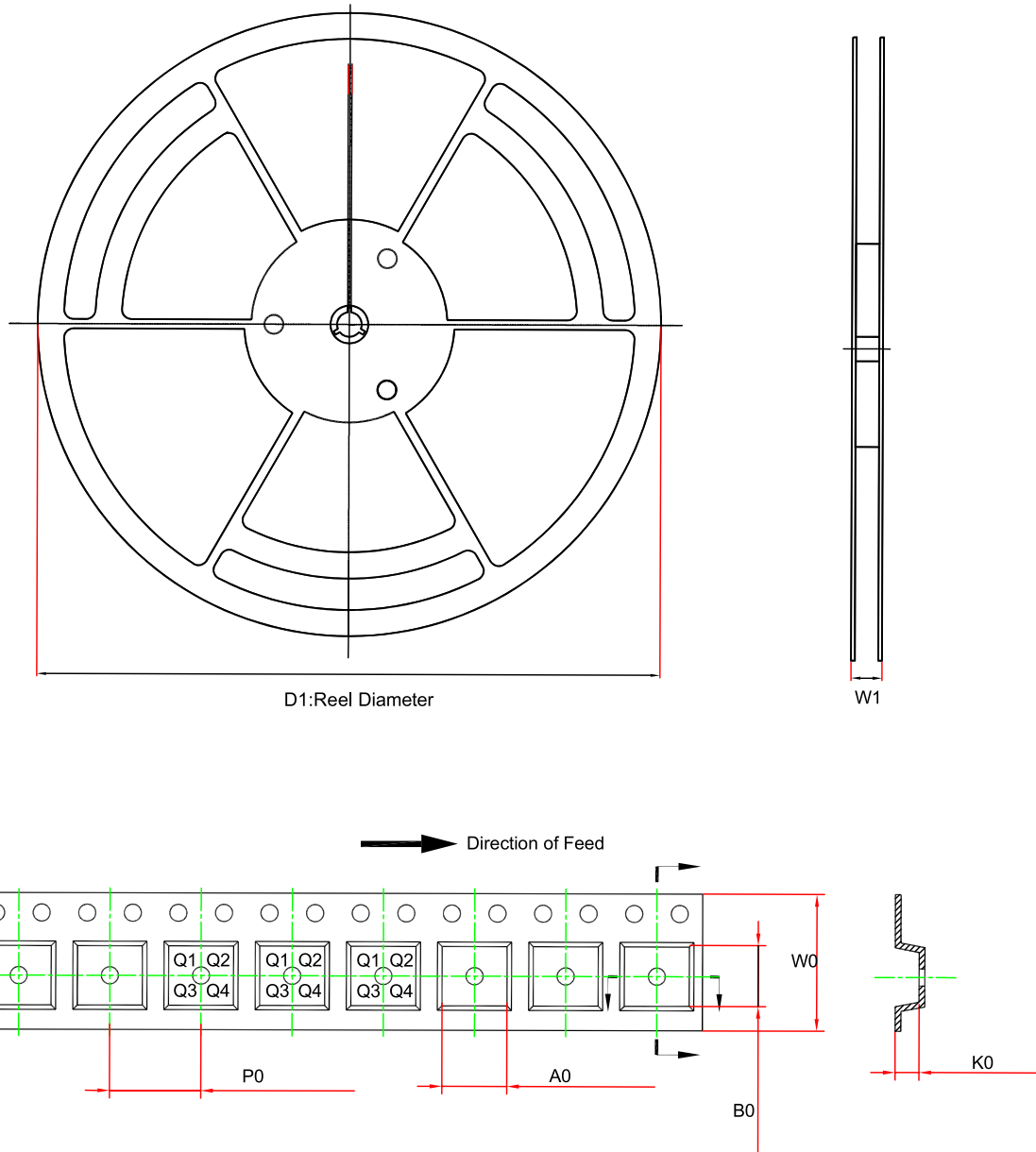


**Figure 21. Bi-Directional Current Sense Amplifier**



**Figure 22. Thermistor Measurement**

## Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) <sup>(1)</sup>	B0 (mm) <sup>(1)</sup>	K0 (mm) <sup>(1)</sup>	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP5531U-CR	SOT353	178	12.1	2.4	2.5	1.2	4	8	Q3
TP5531-TR	SOT23-5	180	12	3.3	3.25	1.4	4	8	Q3
TP5531U-TR	SOT23-5	180	12	3.3	3.25	1.4	4	8	Q3
TP5532-SR	SOP8	330	17.6	6.5	5.4	2	8	12	Q1
TP5532-VR	MSOP8	330	17.6	5.3	3.4	1.3	8	12	Q1
TP5532-FR	DFN2X2-8	180	12.5	2.2	2.2	0.7	4	8	Q1
TP5534-SR	SOP14	330	21.6	6.5	9.3	2.1	8	16	Q1

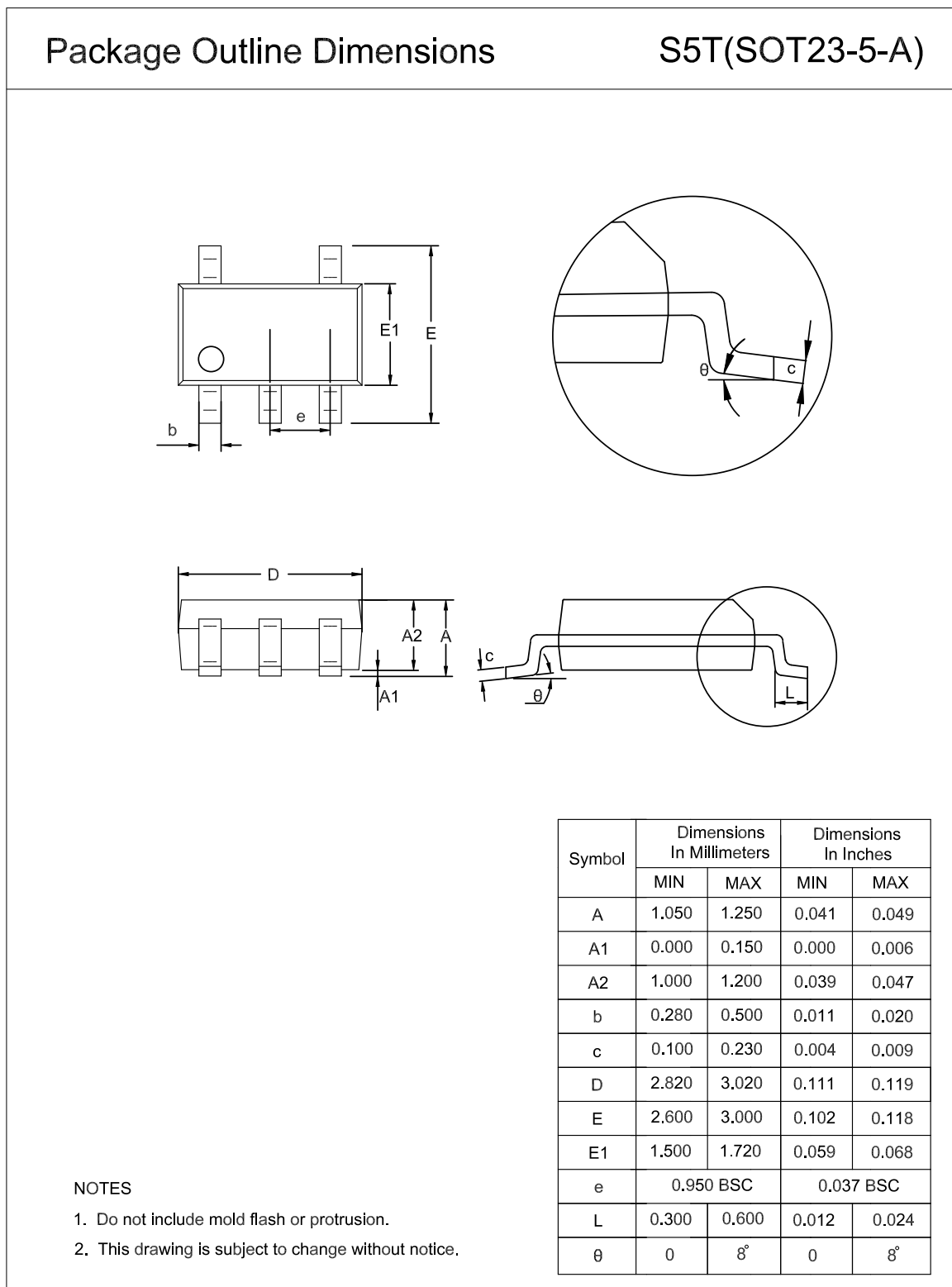
**1.8-V, 42- $\mu$ A, RRIO, Zero-Drift Operational Amplifier**

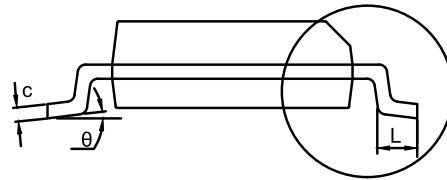
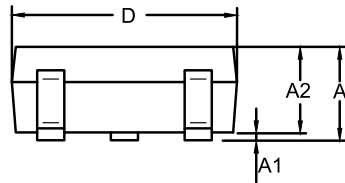
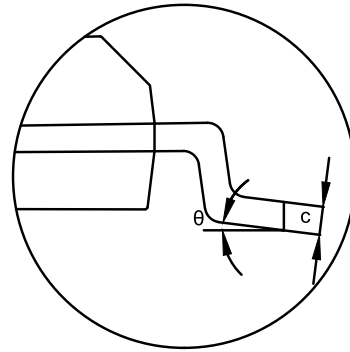
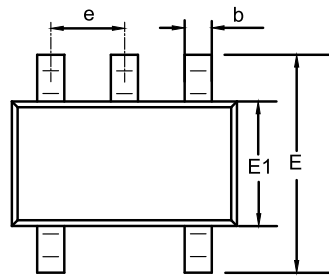
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) <sup>(1)</sup>	B0 (mm) <sup>(1)</sup>	K0 (mm) <sup>(1)</sup>	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP5534-TR	TSSOP14	330	17.6	6.8	5.5	1.5	8	12	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

## Package Outline Dimensions

### SOT23-5

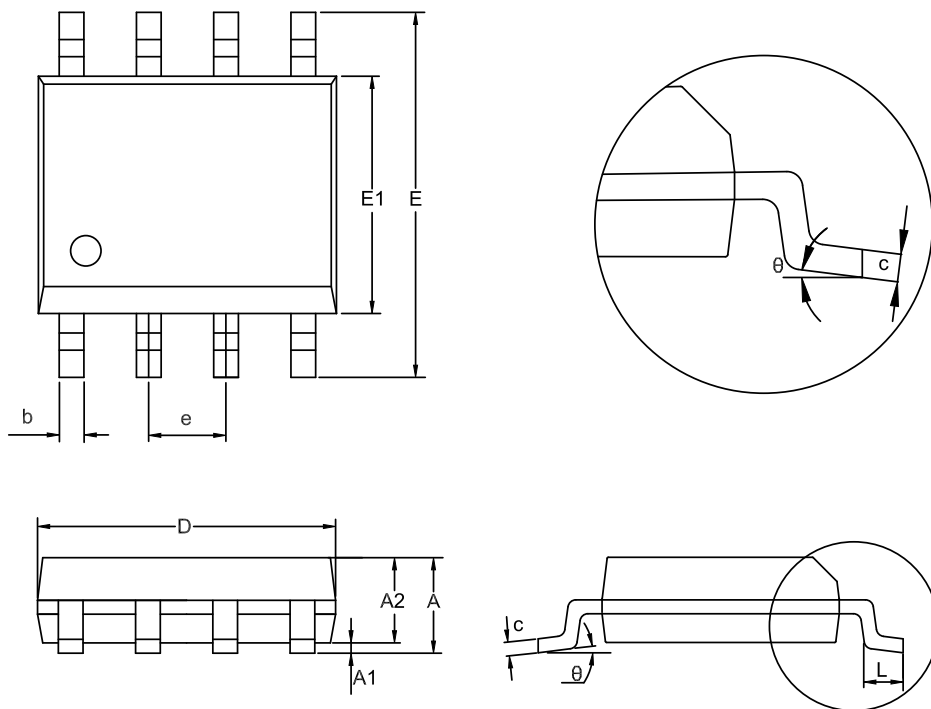


**SOT353 (SC70-5)**
**Package Outline Dimensions**
**SC5(SOT353-5-A)**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.850	1.100	0.033	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.230	0.004	0.009
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 BSC		0.026 BSC	
L	0.260	0.460	0.010	0.018
$\theta$	0	8°	0	8°

**NOTES**

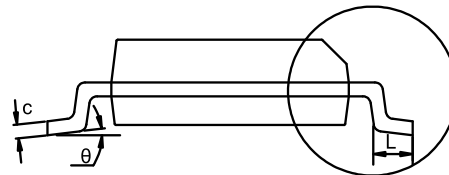
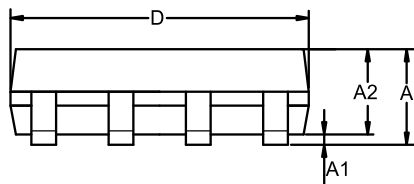
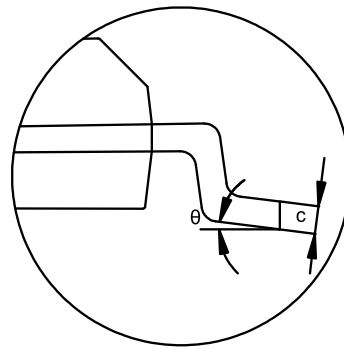
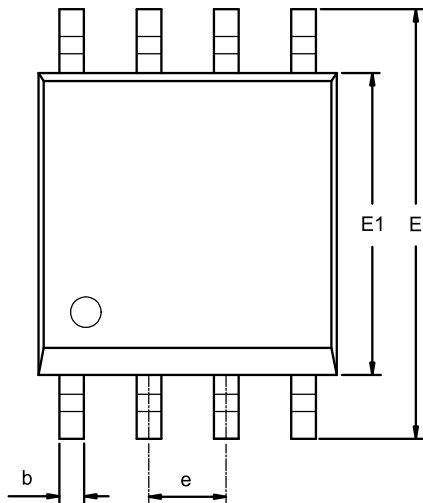
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

**SOP8**
**Package Outline Dimensions**
**SO1(SOP-8-A)**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
$\theta$	0	8°	0	8°

**NOTES**

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

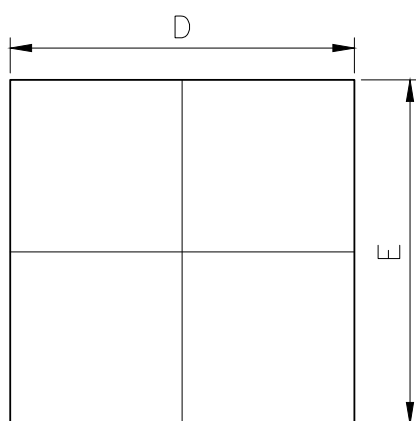
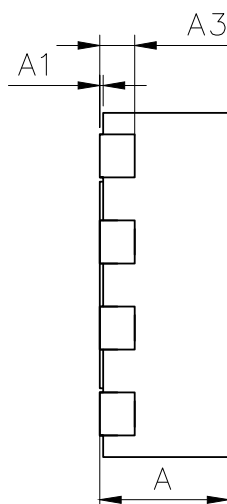
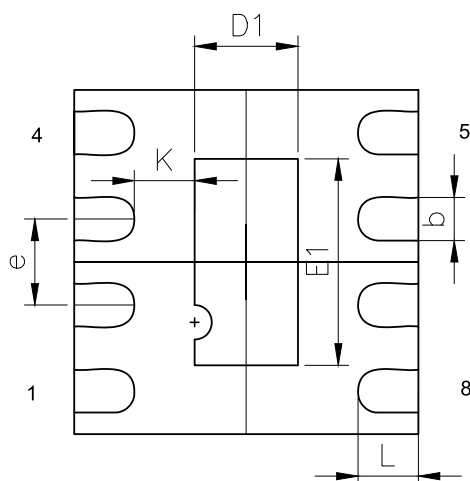
**MSOP8**
**Package Outline Dimensions**
**VS1(MSOP-8-A)**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
$\theta$	0	8°	0	8°

**NOTES**

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

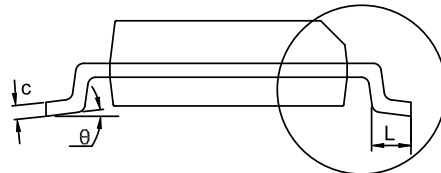
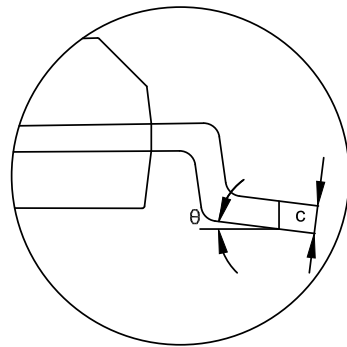
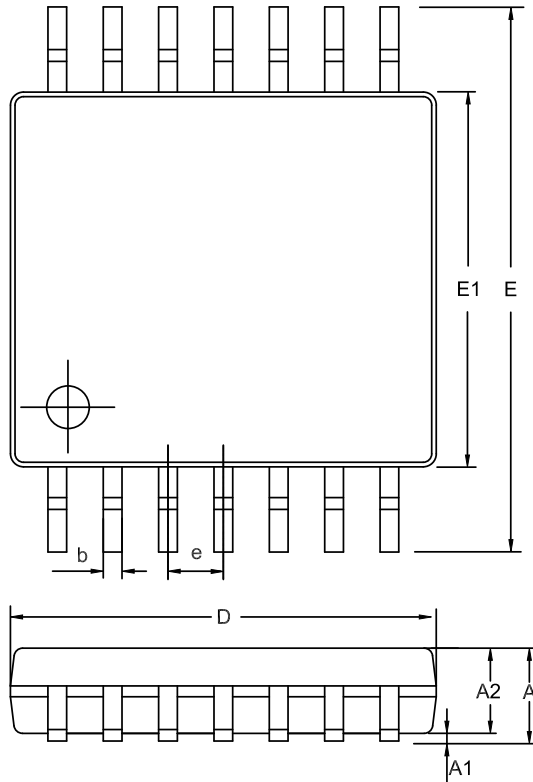


**DFN2X2-8**
**Package Outline Dimensions**
**DF4(DFN2X2-8-A)**

**Top View**

**Side View**

**Bottom View**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
A3	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D1	0.500	0.700	0.020	0.028
E	1.900	2.100	0.075	0.083
E1	1.100	1.300	0.043	0.051
e	0.500 BSC		0.020BSC	
L	0.274	0.426	0.011	0.017

**NOTES**

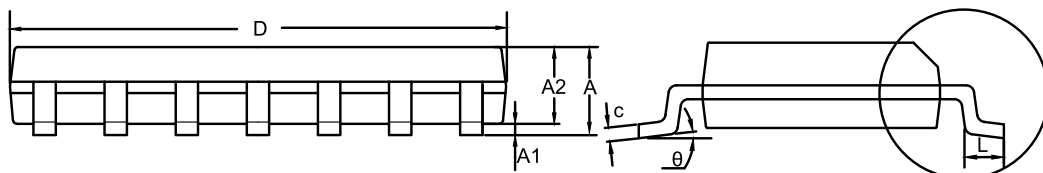
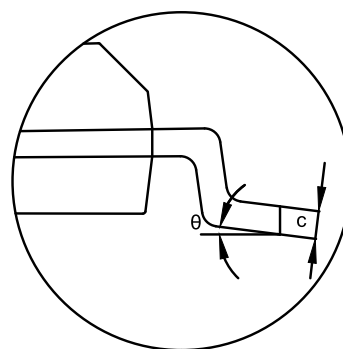
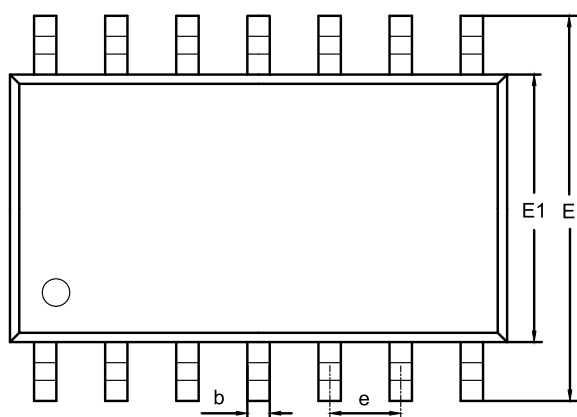
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

**TSSOP14**
**Package Outline Dimensions**
**TS2(TSSOP-14-A)**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
$\theta$	0	8°	0	8°

**NOTES**

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

**SOP14**
**Package Outline Dimensions**
**SO2(SOP-14-A)**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
$\theta$	0	8°	0	8°

**NOTES**

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

## Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TP5531-TR	-40 to 125°C	SOT23-5	E31T	3	Tape and Reel, 3,000	Green
TP5531U-TR	-40 to 125°C	SOT23-5	E31U	3	Tape and Reel, 3,000	Green
TP5531U-CR	-40 to 125°C	SOT353 (SC70-5)	31V	3	Tape and Reel, 3,000	Green
TP5532-SR	-40 to 125°C	SOP8	TP5532	3	Tape and Reel, 4,000	Green
TP5532-FR	-40 to 125°C	DFN2X2-8	532	3	Tape and Reel, 3,000	Green
TP5532-VR	-40 to 125°C	MSOP8	TP5532	3	Tape and Reel, 3,000	Green
TP5534-SR	-40 to 125°C	SOP14	TP5534	3	Tape and Reel, 2,500	Green
TP5534-TR	-40 to 125°C	TSSOP14	TP5534	3	Tape and Reel, 3,000	Green

**Green:** 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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