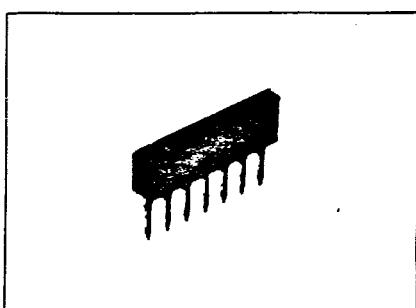


**FM IF Amplifier  
BA402**
**ROHM**

T-74-11-01



The BA402 is a monolithic integrated circuit having a 3-stage differential amplifier used for FM IF amplification and TV sound amplification. The third stage uses an open-collector outputs and has excellent characteristics when used as a limiter circuit. The device is housed in a 7-pin SIP package to save space and enhance ease-of-use.

**Features**

1. High gain.
2. Good limiting characteristics.
3. Large maximum output voltage.
4. Wide frequency range ( $f=1\text{kHz} \sim 20\text{MHz}$ ).
5. Compact SIP package ensures ease-of-use.

**Applications**

FM tuners  
Radios  
Stereos  
Car stereo systems  
TV sound stages

**Absolute Maximum Ratings ( $T_a=25^\circ\text{C}$ )**

Parameter	Symbol	Limits	Unit
Supply voltage	$V_{cc}$	15	V
Power dissipation	$P_d$	$300^*$	mW
Operating temperature range	$T_{opr}$	$-25 \sim 75$	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	$-55 \sim 125$	$^\circ\text{C}$

\* Derating is done at  $3\text{mW}/^\circ\text{C}$  for operation above  $T_a=25^\circ\text{C}$ .

**Electrical Characteristics ( $T_a=25^\circ\text{C}$ ,  $V_{cc}=12\text{V}$ )**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Test circuit
Quiescent current	$I_q$	—	11	15	mA	—	Fig. 9
Output current	$I_{out}$	—	2.5	—	mA	—	Fig. 9
Closed loop voltage gain	$G_{vc}$	54	60	—	dB	With a load capacitance of $13\text{pF}$ and $f=10.7\text{MHz}$	Fig. 10
Input impedance	$R_{IN}$	—	5	—	k $\Omega$	$f=1\text{MHz}$	Fig. 11
Input capacitance	$C_{IN}$	—	5	—	pF	$f=1\text{MHz}$	Fig. 11
Output impedance	$R_{out}$	—	10	—	k $\Omega$	$f=1\text{MHz}$	Fig. 12
Output capacitance	$C_{out}$	—	5	—	pF	$f=1\text{MHz}$	Fig. 12
Input limiting voltage	$V_{in}(\text{lim})$	—	600	—	$\mu\text{V}$	$f=10.7\text{MHz}$ (Fig. 7)	Fig. 10

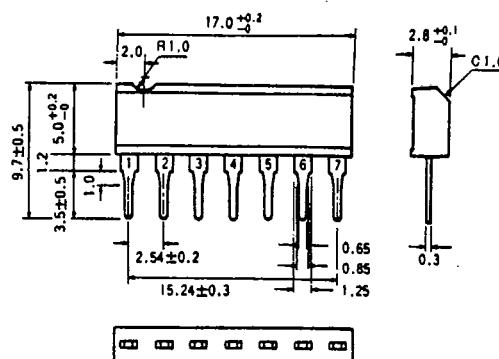
**Dimensions (Unit: mm)**

Fig. 1

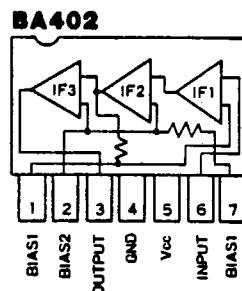
**Block Diagram**

Fig. 2

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## Electrical Characteristic Curves

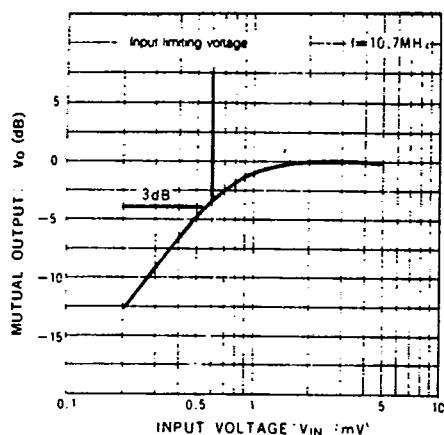


Fig. 3 Input limiting characteristics

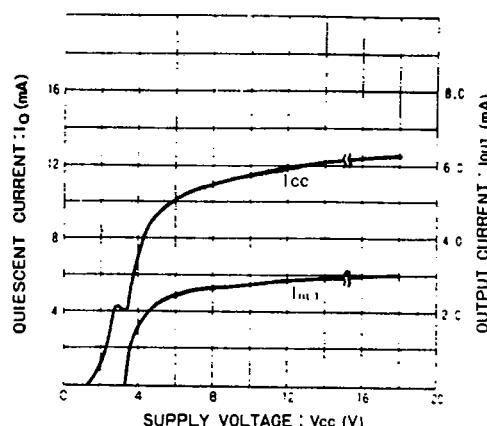


Fig. 4 Quiescent and output currents vs. supply voltage

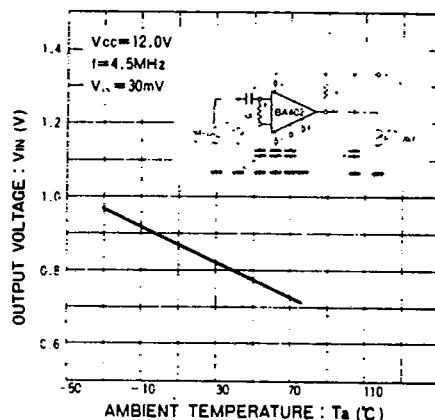


Fig. 5 Output voltage vs. ambient temperature

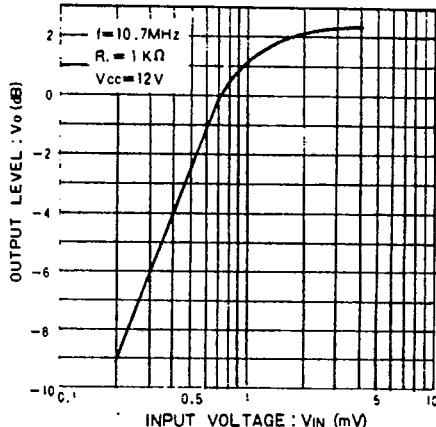


Fig. 6 Output level vs. input voltage

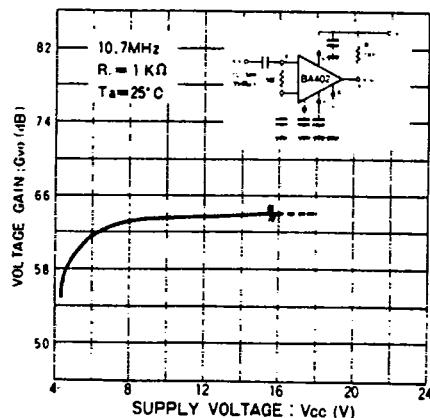


Fig. 7 Voltage gain vs. supply voltage

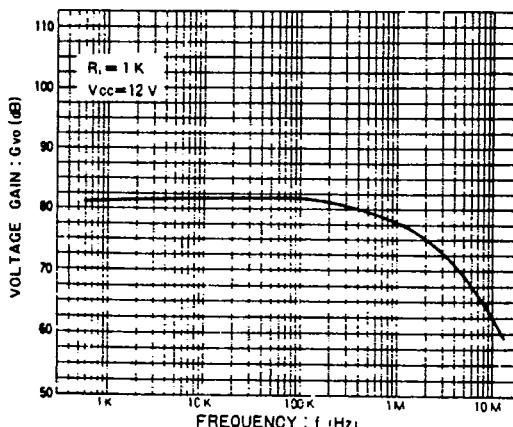


Fig. 8 Voltage gain vs. frequency

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## Test Circuit

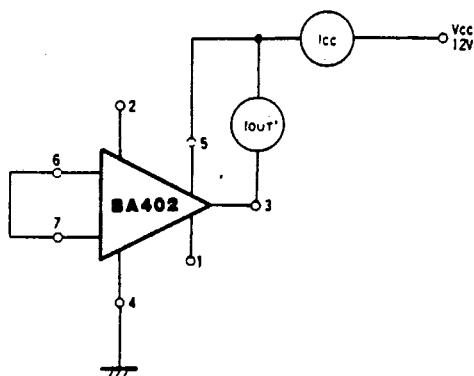


Fig. 9 Test circuit for supply current and output current

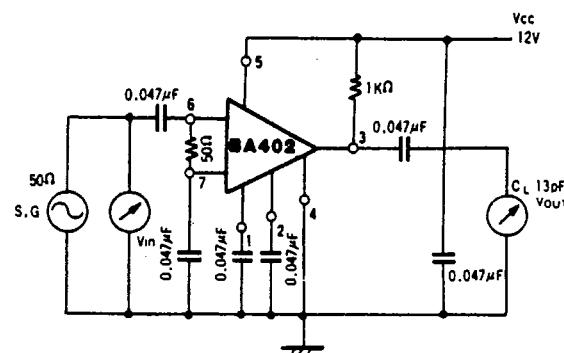


Fig. 10 Test circuit for voltage gain and input limiting voltage

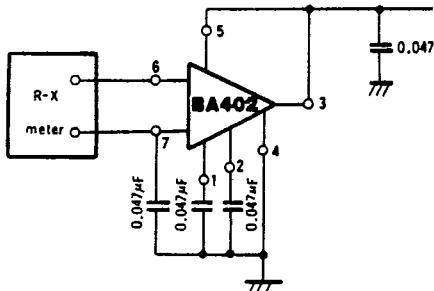


Fig. 11 Test circuit for input impedance and input capacitance

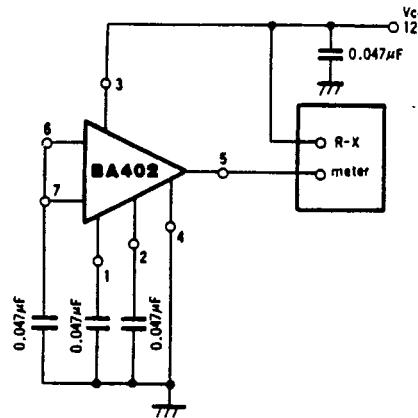


Fig. 12 Test circuit for output impedance and capacitance

## Circuit Description

As shown in Fig. 13, BA402 consists of a 3-stage differential amplifier and bias circuit. The output of the third stage of the amplifier is open-collector configured and operates as a limiter. The bias voltage of the differential amplifier is 3V<sub>BE</sub>.

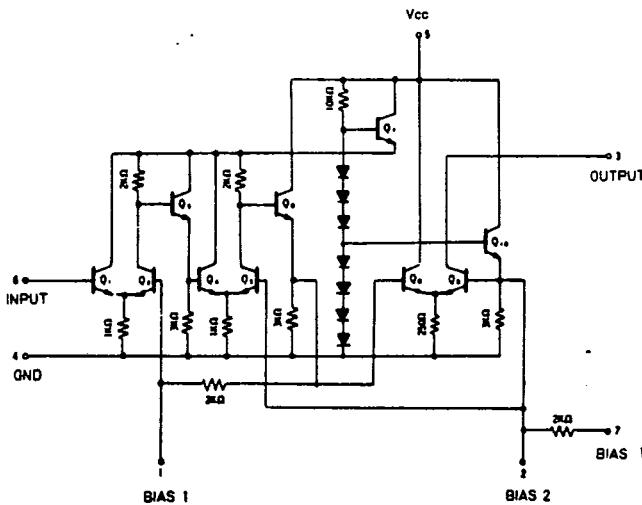


Fig. 13 BA402 internal equivalent circuit

## Application Example

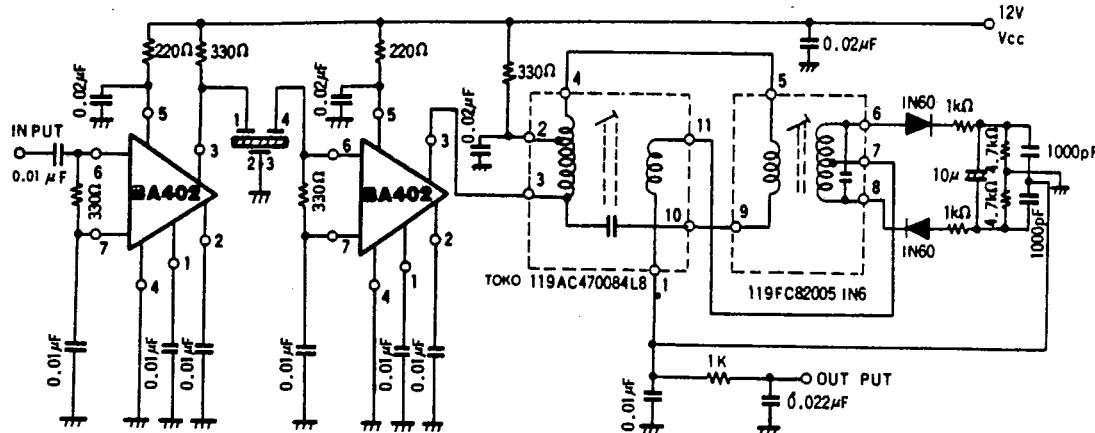


Fig. 14

### External Components

1. Input Coupling Capacitor (Pin 6)  
This is an interstage coupling capacitor between IF amplifier stages.
2. Input Bias Resistor (Pins 6 and 7)  
This resistor provides bias voltage to pin 6 and performs impedance matching.
3. Bias Capacitor (Pins 1, 2, and 7)  
These capacitors stabilize the bias voltage.
4. Output Resistor (Pin 3)  
This resistor forms the load resistance for the differential amplifier.
5. Output Coupling Capacitor (Pin 3)  
This capacitor is the coupling capacitor to the next stage.

### Precautions for Use

#### Notes on PC Board Wiring:

Since this amplifier has a high gain of 60dB at 10.7MHz, special attention is required with regard to printed circuit layout. The following precautions are recommended.

1. Connect the bias capacitor between pins 1 and 4.
2. Ground the decoupling capacitor in the supply line so that the biased signal does not affect the BA402 input.
3. Patterns should be laid out so that the input and output circuits are not coupled. This is particularly true of the 2-stage cascade configuration.

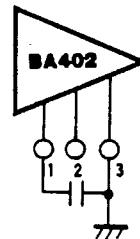


Fig. 15