

**LA3246**

Stereo Preamplifier for Compact Double Cassette Playback-only Use

Overview

The LA3246 is a stereo preamplifier IC for double cassette tape playback-only use. The LA3246 is intended for use in portable radio-cassette tape recorders and tape decks.

Applications

- Stereo compact cassette player for playback-only use
- Stereo cassette deck player

Functions

- Preamplifier × 2, Mixing amplifier × 1, Electronic switch × 6

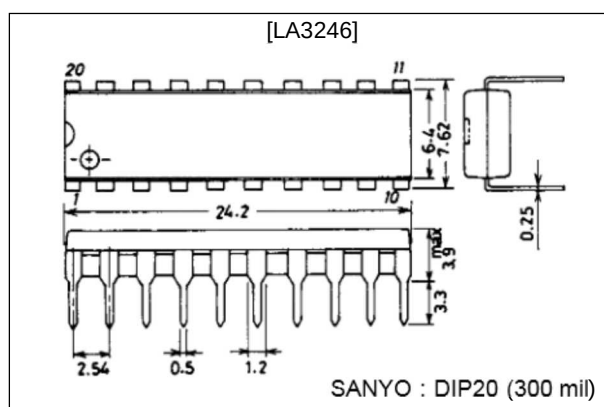
Features

- On-chip electronic switch for input select (auto reverse or A deck/B deck select)
- On-chip electronic switch for normal/higher dubbing select and electronic switch for metal/normal tape select
- Wide operating voltage range ($V_{CC\text{ op}} = 3.5$ to 14 V)
- With output MIX pin (for music select control)
- Low noise voltage range ($V_{NI} = 0.9\text{ }\mu\text{V typ}$, $R_g = 2.2\text{ k}\Omega$ NAB)
- Can be used in conjunction with the LA3240, 3241, 3242 to easily make up a doublecassette dubbing system.

Package Dimensions

unit : mm

3021B-DIP20



Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		16	V
Allowable power dissipation	$P_d\text{ max}$		500	mW
Operating temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		6	V
Operating voltage range	$V_{CC\text{ op}}$		3.5 to 14	V

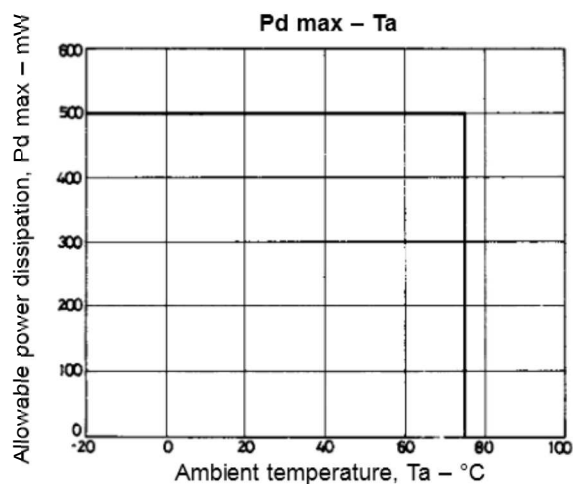
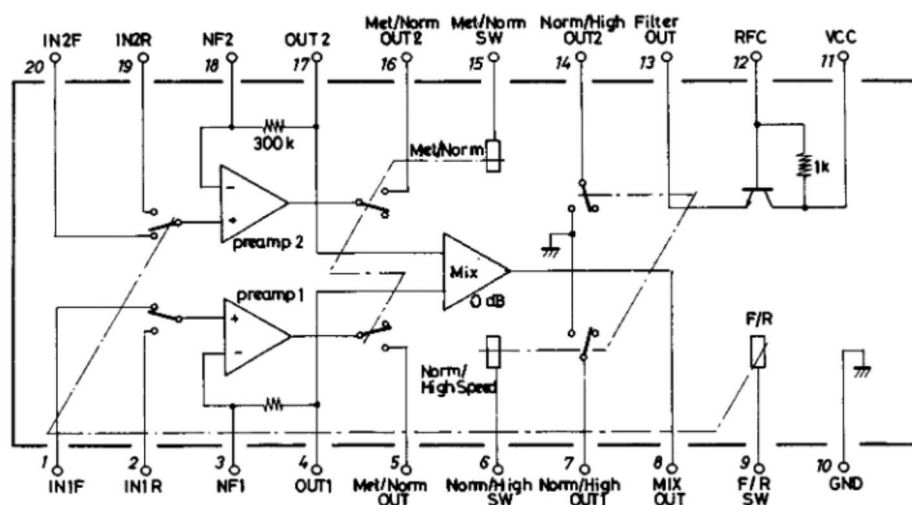
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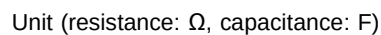
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

D3097HA(II)/41594HK/N107TA, TS No.2651-1/13

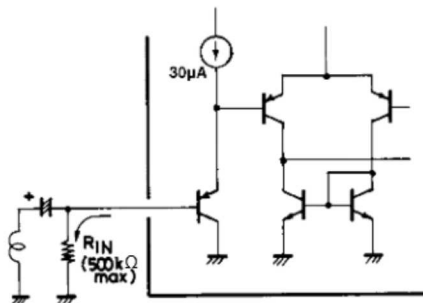
Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 6.0\text{ V}$, $R_L = 10\text{ k}\Omega$, $f = 1\text{ kHz}$, $0\text{ dB} = 0.775\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	I _{cco}	Nor/Nor speed forward	5	7	12	mA
	I _{ccs}	Metal/High speed forward	7	10	17	mA
Voltage gain (Open)	V _{Go}		75	85		dB
Voltage gain (Closed)	V _G	Nor/Nor speed, NAB	39.5	40.5	41.5	dB
Total harmonic distortion	THD	V _O = 0.65 V, Nor/Nor speed		0.03	0.2	%
Maximum output voltage	V _O max	THD = 1%, Nor/Nor speed	0.7	1.2		V
Crosstalk (between channels)	CT1	V _O = -5 dBm, R _g = 2.2 k Ω , Nor/Nor speed	50	65		dB
Crosstalk (between F/R)	CT2	V _O = -5 dBm, R _g = 2.2 k Ω , Nor/Nor speed	50	65		dB
Channel balance	V _{BL}	V _{IN} = -50 dBm		0	2	dB
Equivalent input noise voltage	V _{NI}	R _g = 2.2 k Ω , B.P.F 20 Hz to 20 kHz, Nor/Nor speed		0.9	1.7	μV
MIX output voltage	V _O MIX	V _{O1} , V _{O2} = 0 dBm	-3	0	+3	dB
Ripple filter output current	I _F OUT			10	15	mA
Electronic switch ON-state resistance	R _{on}	Between P1 to P4 and 5, between pin 16 and 17		100	250	Ω
		Between P1 to P7 and 10, between pin 10 and 14		30	70	Ω
DC feedback resistance	R _F		240	300	360	Ω
Input bias current	I _F			0.5	3.0	μA


Equivalent Circuit Block Diagram


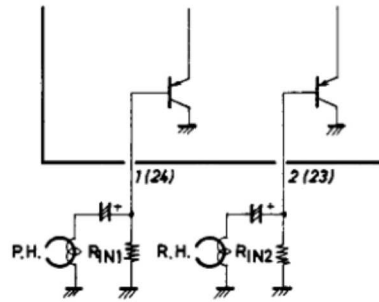


- (1) It is recommended to connect a surge absorbing capacitor across input pins 1, 2 and GND and across input pins 19, 20 and GND.
- (2) The base of a PNP transistor is connected to input pins 1, 2 and 19, 20. If an electrolytic capacitor is connected in series with the input pins, connect input resistor R_{IN} must not exceed 500 k Ω . (Reason: To minimize the variation in output DC voltage at the time of input switching)



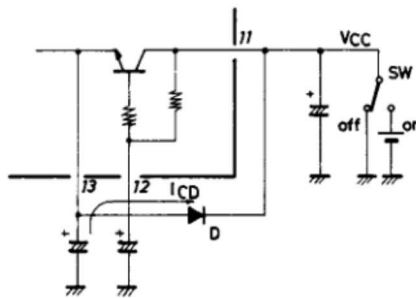
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- (3) When an electrolytic capacitor is connected to input pins 1, 2 (or 23, 24), make the value of R_{IN1} as equal to that of R_{IN2} as possible.

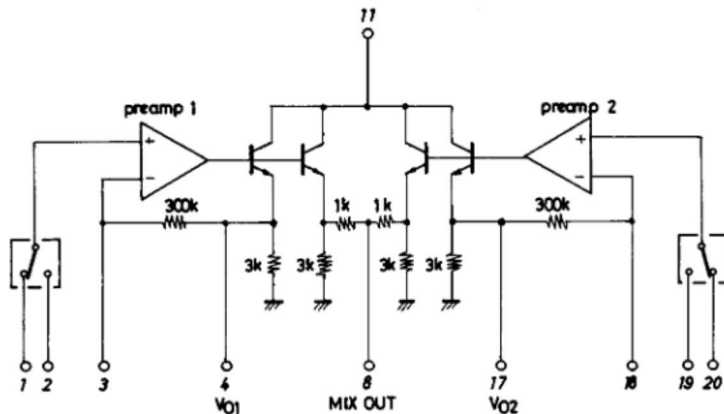


The difference in the value between R_{IN1} and R_{IN2} causes the variation in amp output DC voltage at the time of F/R switching. Therefore, the input DC voltage (voltage across R_{IN}) must be made as equal as possible.

- (4) The amplifier output characteristics are designed to be the same in the Nor Tape/High Speed (pin 15 GND/pin 6 V_{CC}) and Me Tape/Nor Speed (pin 15 V_{CC} /pin 6 GND) modes. (Refer to sample application circuit, external constants.)
- (5) When externally turning ON/OFF power supply pin 11 (by bringing pin 11 to $+V_{CC}$ /GND level) with a capacitor connected to pin 13, connect external diode D, as shown below, so that no breakdown (or deterioration) of the IC system is caused by I_{CD} when the switch is turned OFF. When no capacitor is connected to pin 13, diode D is not required.



- (6) The output MIX circuit is of the emitter follower configuration as shown below.



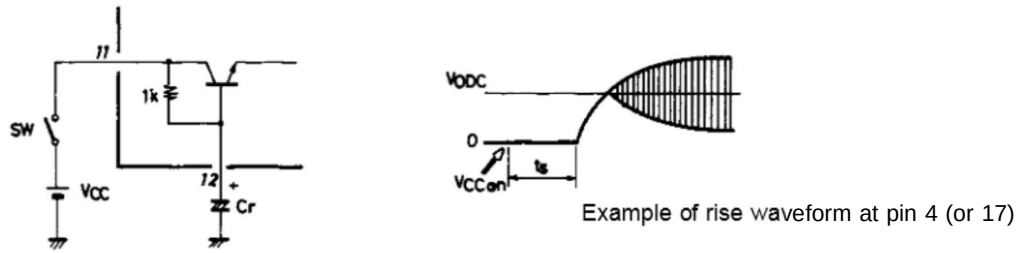
Unit (resistance: Ω)

The MIX OUT output level V_O MIX at the time a signal is applied to preamp1 (or preamp2) only is 1/2 as compared with output levels V_{O1} , V_{O2} at the time the same input signal is applied to both channels.

$$V_O \text{ MIX} = 1/2 \quad V_{O1} (= 1/2 \times V_{O2})$$

where $V_{O1} = V_{O2}$

(7) Output waveform starting time



When supply voltage V_{CC} is switched ON, the amplifier output (pins 4, 17) will rise. Output waveform ON time t_s can be varied by capacitor C_r connected to pin 12.

Refer to Data $C_r - t_s$.

The minimum value of C_r is 47 μF .

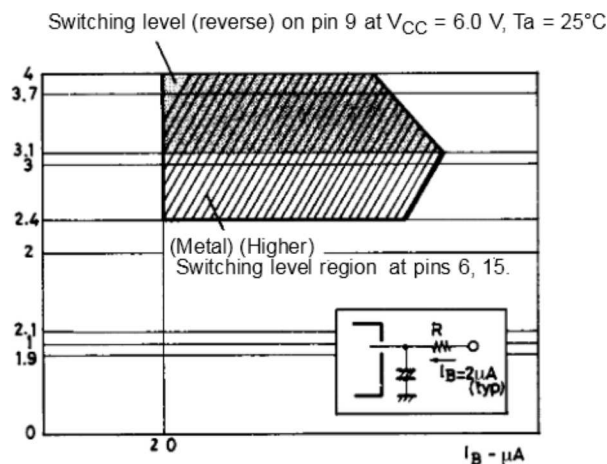
(8) Electronic select switching level

- The switch level at $V_{CC} = 6.0$ V is shown below.

Pin	Switch Mode	Switching Level		Clamp Voltage	Control Current typ (flow-in) (at operation finish)	Mode	
		Operation Start	Operation Finish			(+)	(-)
6	Normal/Metal	2.1 V	2.4 V	3.7 V	2 μA	Metal	Normal
9	Forward/Reverse	2.1 V	3.1 V	3.4 V	2 μA	Reverse	Forward
15	Normal/Higher	2.1 V	2.4 V	3.7 V	2 μA	Higher	Normal

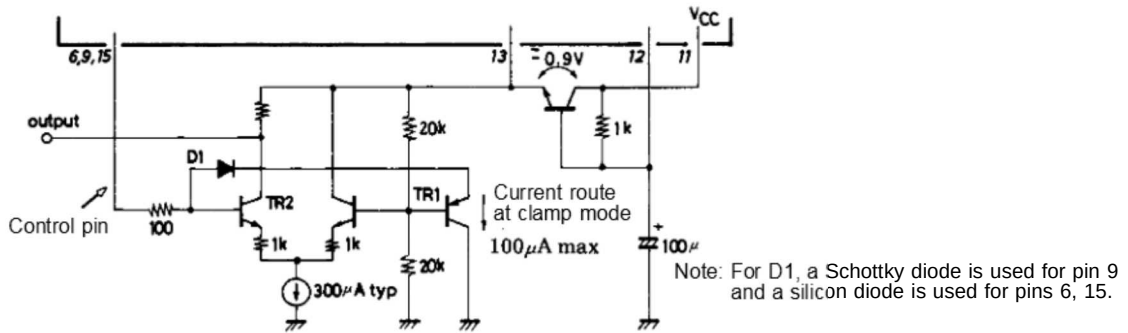
As shown above, there is a difference in the switching level at three control pins (6, 9, 15) between operation start and operation finish.

- Switching level and mode at each pin (experimental value)



• Control circuit

The control circuit for each CONT pin is configured as shown below. When a voltage more than a given value is applied, the level on the pin is fixed by clamp diode D1.



Unit (resistance: Ω, capacitance: F)

Description

- Switching level V_{SW} of the control circuit is fixed by voltage V_{13} which is 1/2 of the voltage on pin 13.

$$V_{SW} = 1/2 V_{13}$$

- Clamp voltage V_{CLP} at the time a voltage is applied to the CONT pin

$$\begin{aligned} V_{CLP} &= 1/2 \times V_{13} + V_{D1} + V_{BE1} \\ &= 1/2 \times V_{13} + 0.6 (0.3) + 0.6 \\ &= 1/2 \times V_{13} + (0.9 \text{ or } 1.2) \end{aligned}$$

where 0.9 V is for pin 9.
1.2 V is for pins 6, 15.

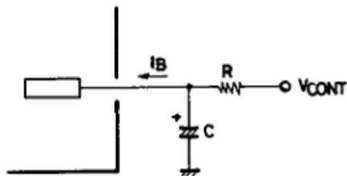
- The maximum voltage at which the CONT pin is brought to GND level is fixed by the level at which the Q2 is completely turned OFF.

This level is:

$$1/2 \times V_{13} - V_{BE2} = 1/2 \times V_{13} - 0.6 \text{ [V]}$$

Switching is performed at a level less than this.

- To turn ON/OFF
When turning ON:



To turn ON the control circuit to finish the operation, I_B is required. Control voltage V_{OUT} is obtained with I_B of 4 μA min.

- $V_{CONT \text{ min}} = R \times I_B \text{ max} + \text{Operation finish voltage.}$

$$I_B = 4 \mu\text{A}$$

Operation finish voltage

$$\text{Pins 6, 15 : } = 1/2 \times V_{13}$$

$$\begin{aligned} \text{Pin 9 : } &= 1/2 \times V_{13} + V_{BE} \\ &= 1/2 \times V_{13} + 0.6 \text{ [V]} \end{aligned}$$

- $V_{CONT \text{ max}} = R \times I_B \text{ max} + \text{Clamp voltage}$
 R is restricted by $I_B \text{ max.}$

When the supply voltage is fixed, clamp voltage V_{CLP} is fixed. When resistor R is fixed based on a balance with capacitor C , resistor R is restricted by $V_{CONT \text{ max.}}$ as shown below.

$$I_B \text{ max} = 100 \mu\text{A} \wedge \frac{V_{CONT \text{ max}} - V_{CLP}}{R}$$

The minimum value of resistor R is fixed by this equation.

Example

Assuming $V_{CC} = 10 \text{ V}$, $V_{CONT \text{ max}} = 10 \text{ V}$, R_{min} is 50 kΩ.

Therefore, $R = 100 \text{ k}\Omega$ presents no problem.

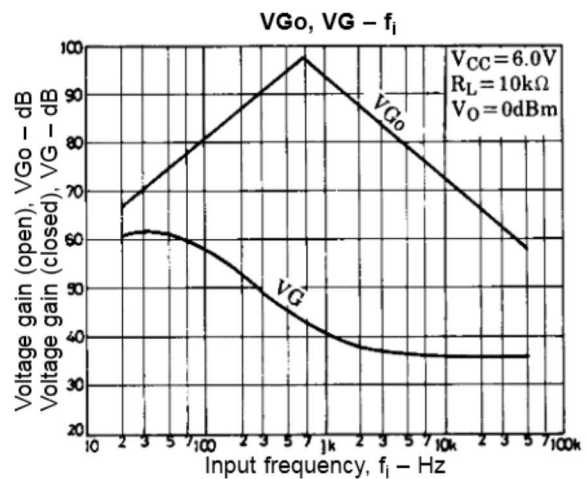
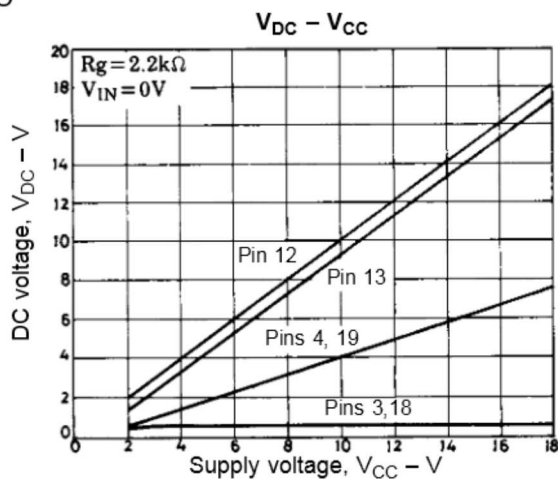
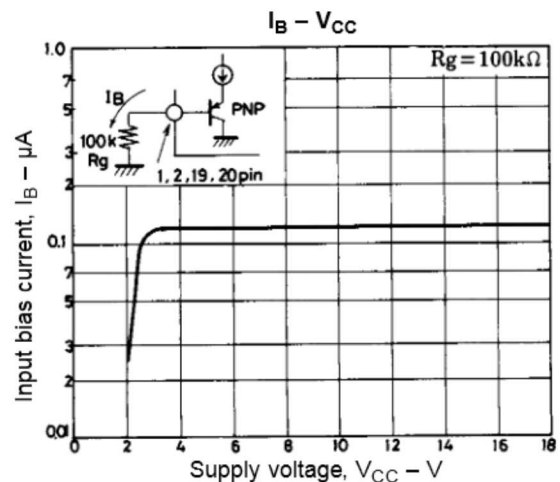
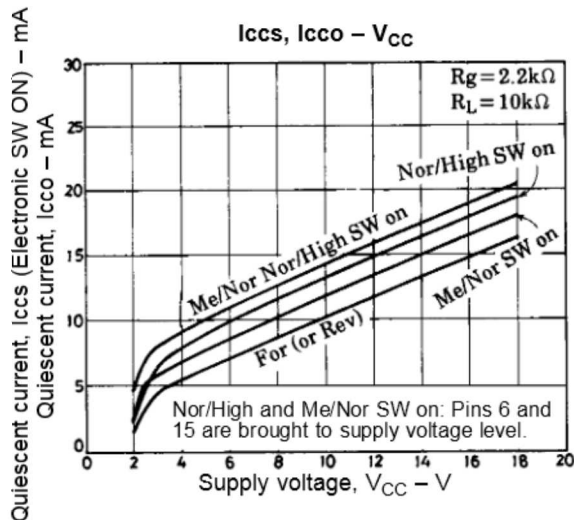
When turning OFF:

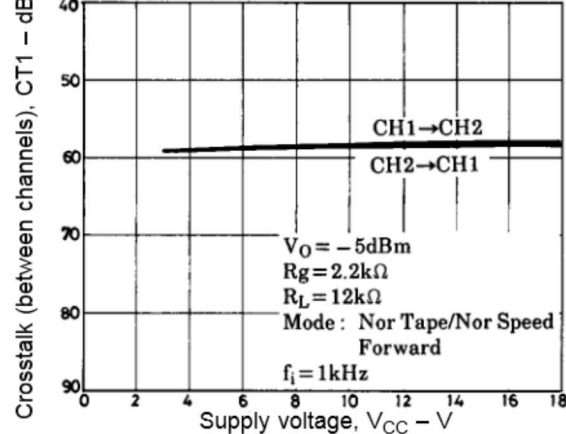
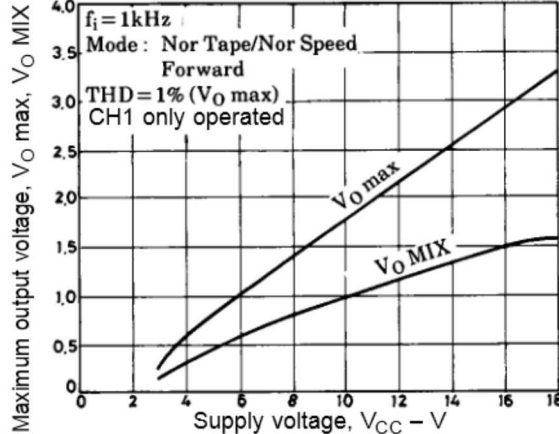
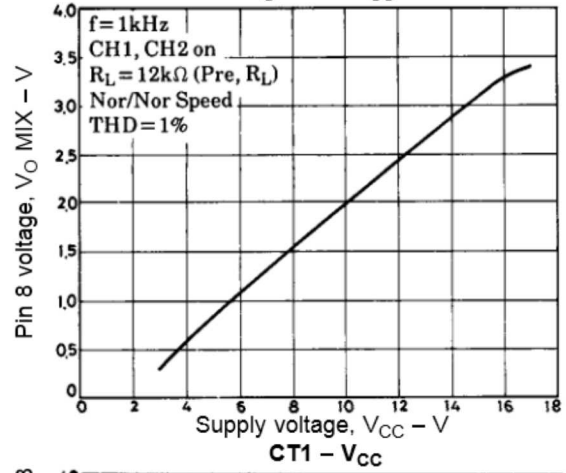
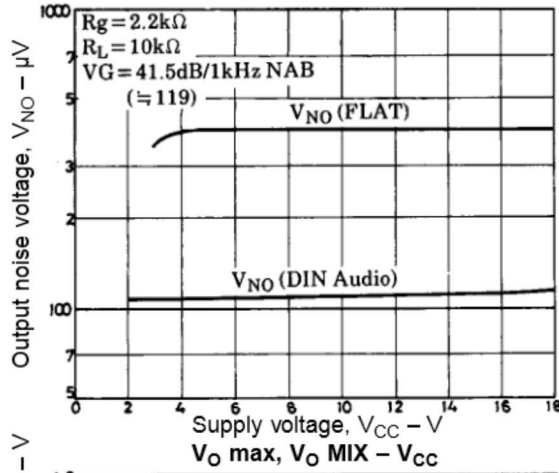
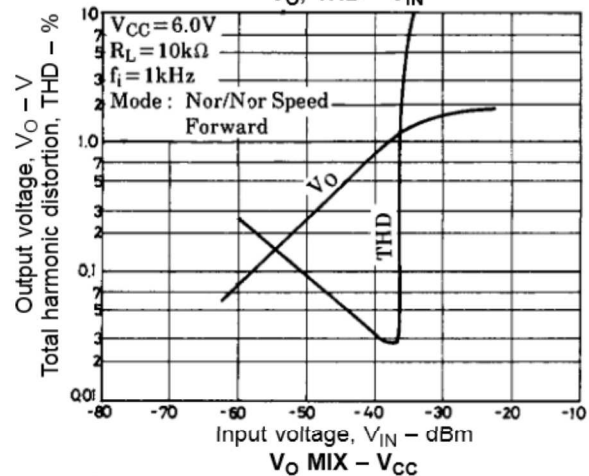
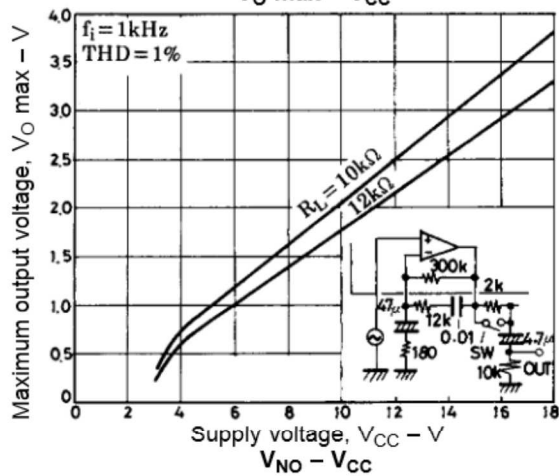
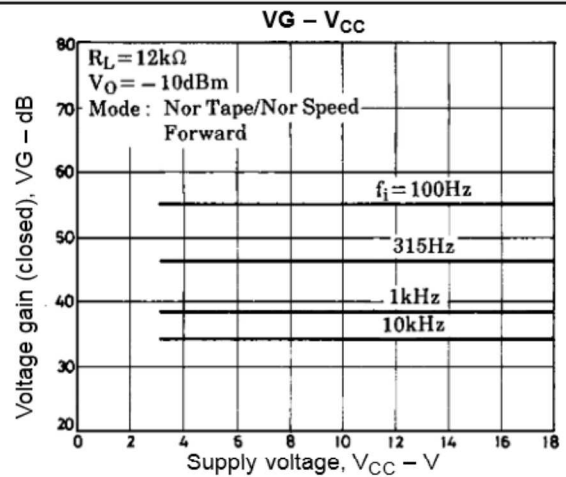
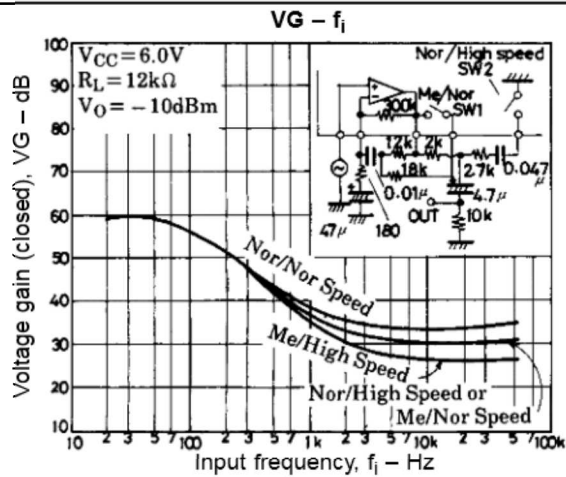
Bring the level on the CONT pin to a level less than:

$$1/2 \times V_{13} - V_{BE2} = 1/2 \times V_{13} - 0.6 \text{ [V]}$$

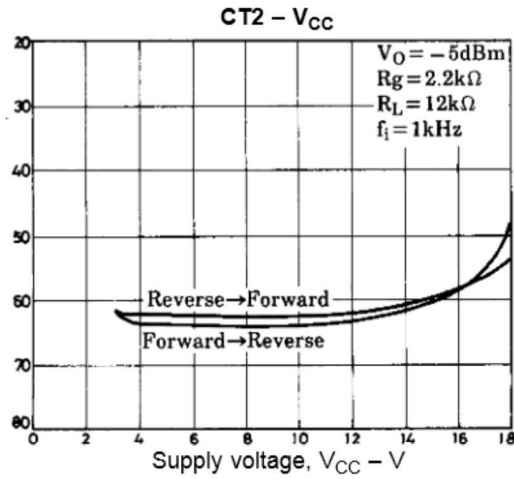
(9) Example of voltage on each pin

Pin	Supply voltage, $V_{CC} - V$				Unit
	4.5 V	6.0 V	9.0 V	12.0 V	
1	0.3	0.3	0.3	0.3	mV
2	0.3	0.3	0.3	0.3	mV
3	0.59	0.58	0.57	0.56	V
4	1.63	2.23	3.65	5.02	V
5	1.63	2.23	3.65	5.02	V
6	(GND) 0	(GND) 0	(GND) 0	(GND) 0	V
7	0	0	0	0	V
8	1.63	2.29	3.64	5.01	V
9	(GND) 0	(GND) 0	(GND) 0	(GND) 0	V
10	(GND) 0	(GND) 0	(GND) 0	(GND) 0	V
11	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V
12	4.48	5.96	8.97	11.23	V
13	3.72	5.20	8.21	11.98	V
14	0	0	0	0	V
15	(GND) 0	(GND) 0	(GND) 0	(GND) 0	V
16	1.63	2.23	3.65	5.02	V
17	1.63	2.23	3.65	5.02	V
18	0.59	0.58	0.57	0.56	V
19	0.3	0.3	0.3	0.3	mV
20	0.3	0.3	0.3	0.3	mV

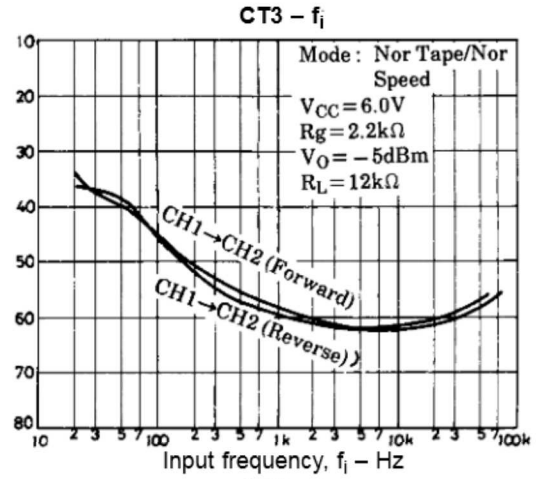




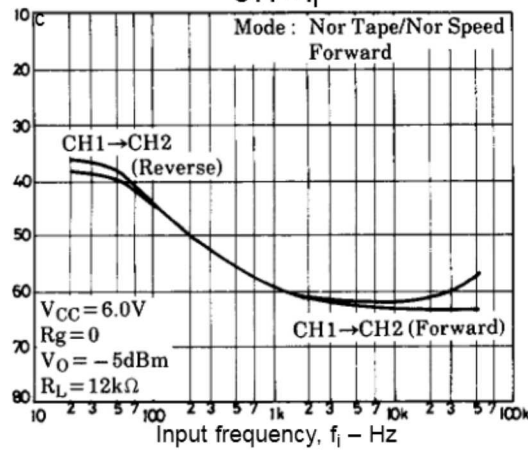
Crosstalk (between forward and reverse), CT2 – dB



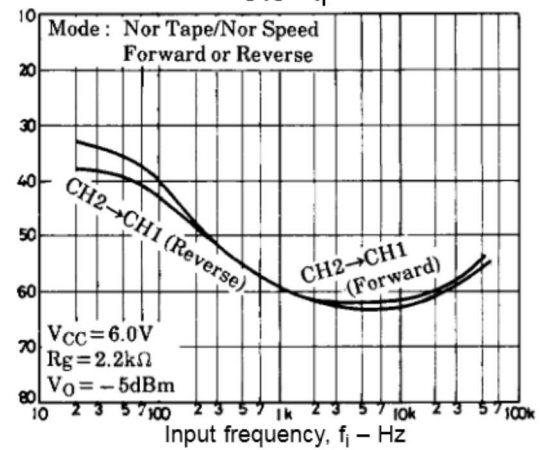
Crosstalk (between channels), CT3 – dB



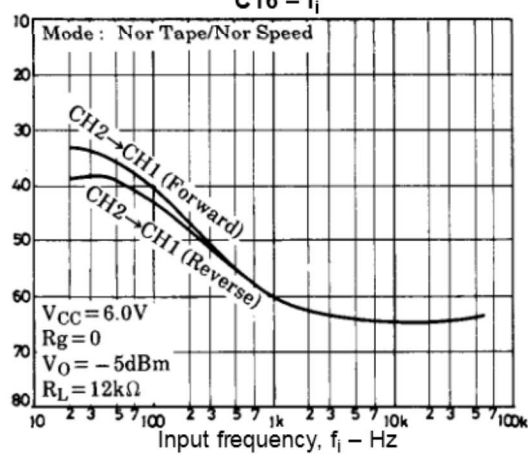
Crosstalk (between channels), CT4 – dB



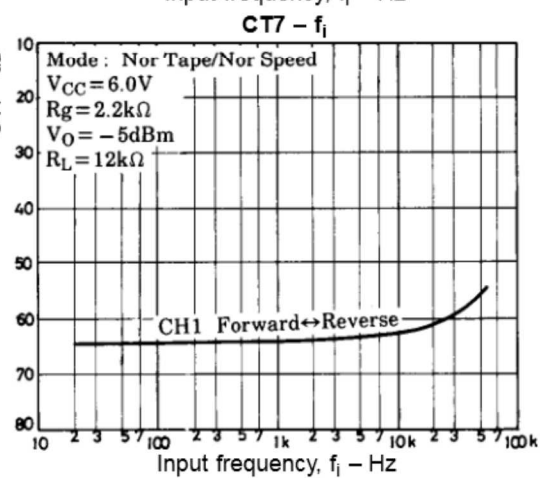
Crosstalk (between channels), CT5 – dB



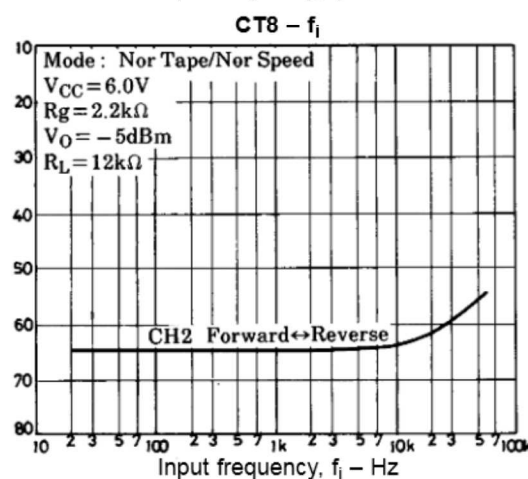
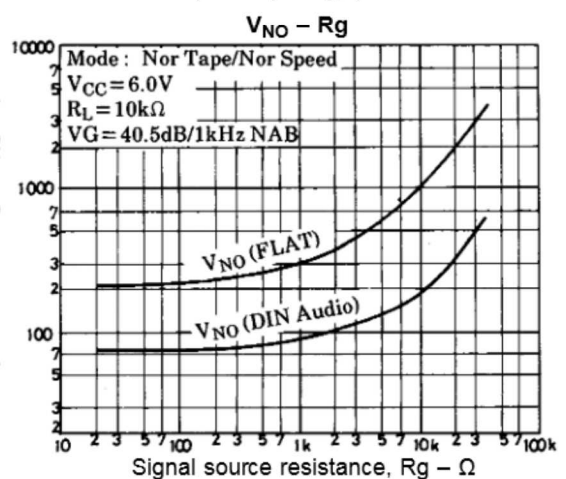
Crosstalk (between channels), CT6 – dB

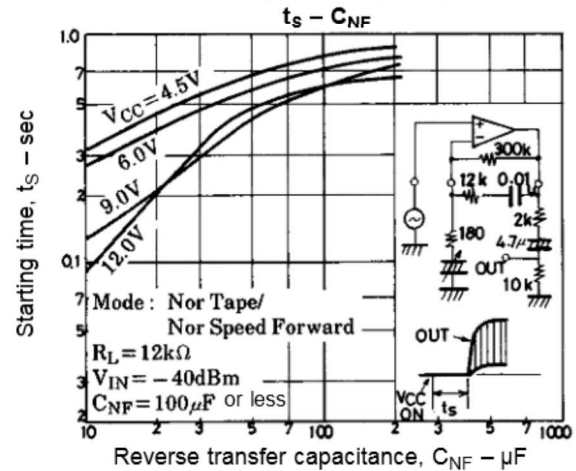
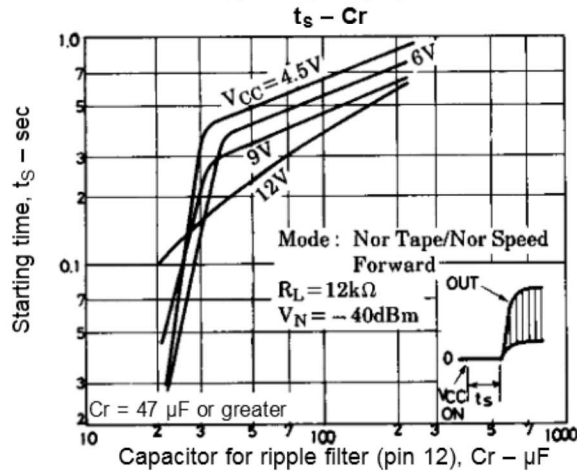
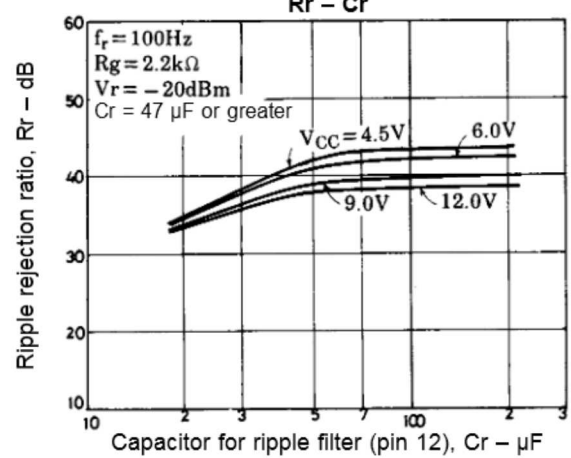
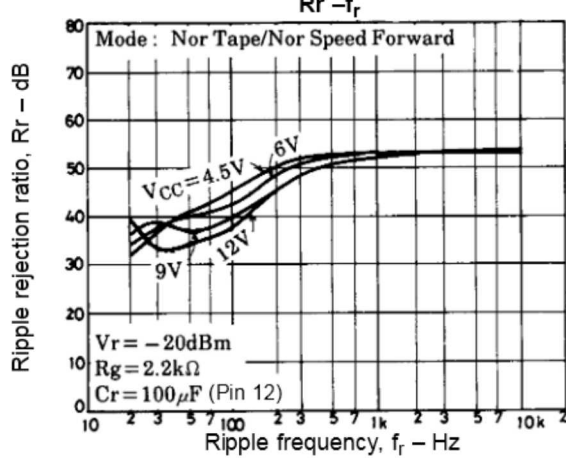
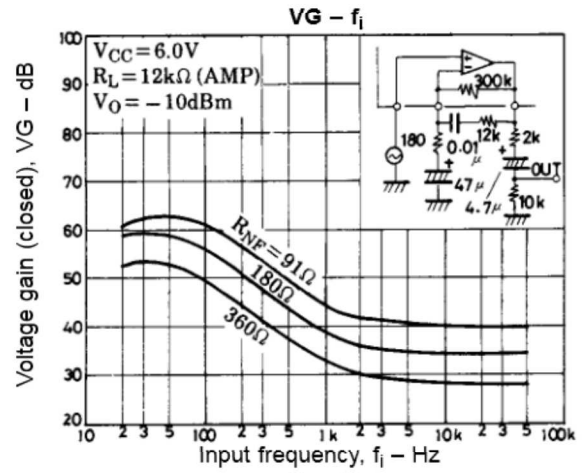
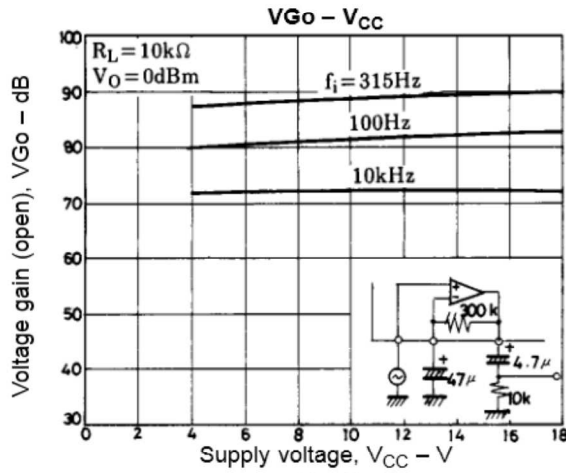
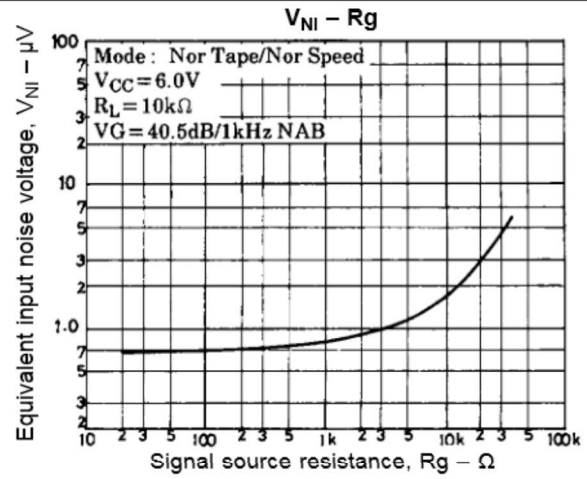
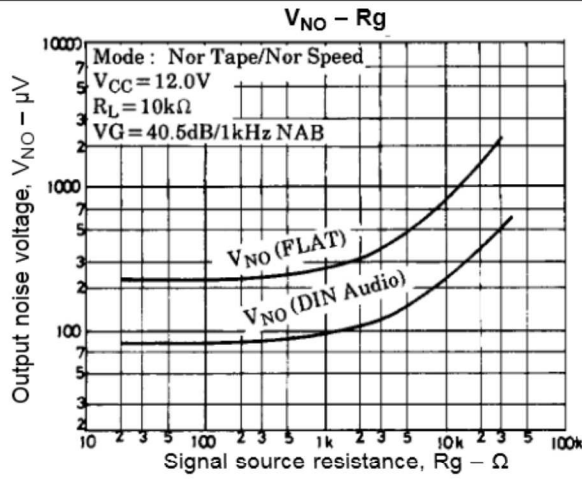


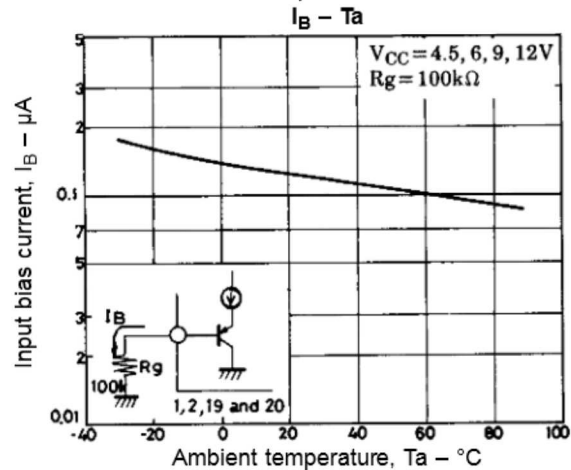
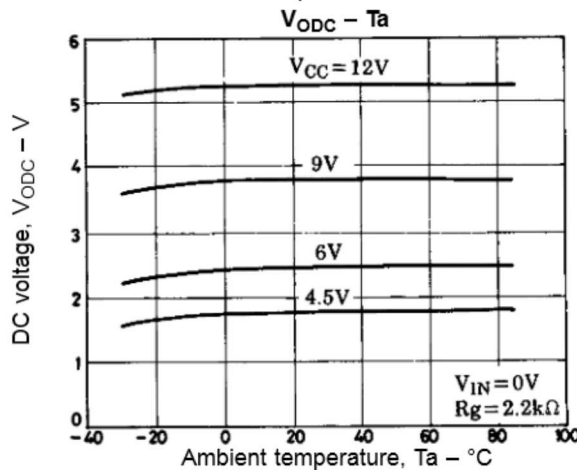
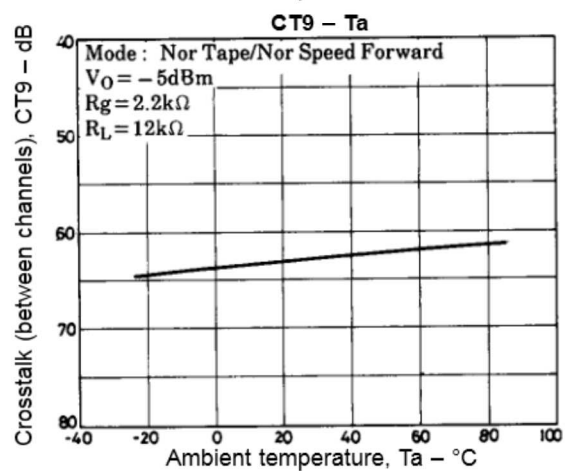
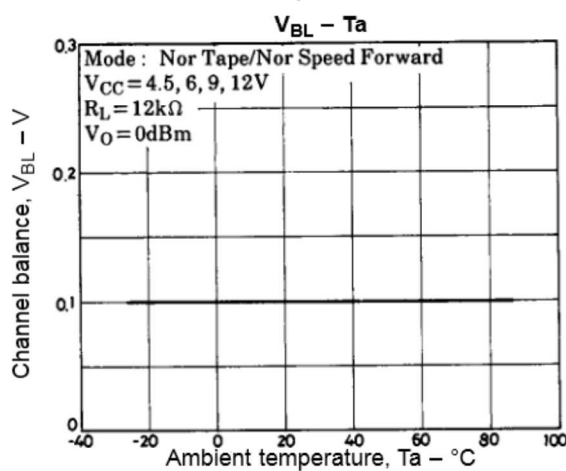
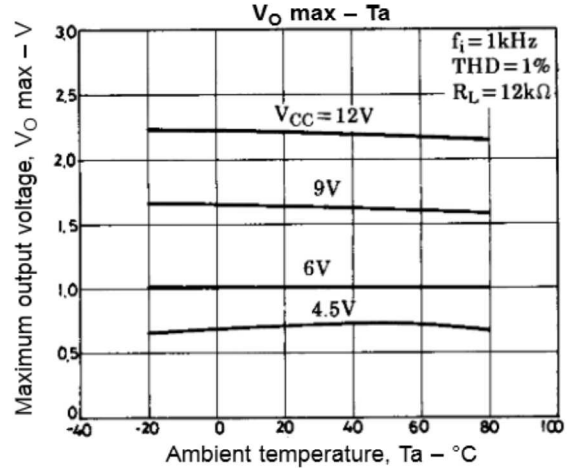
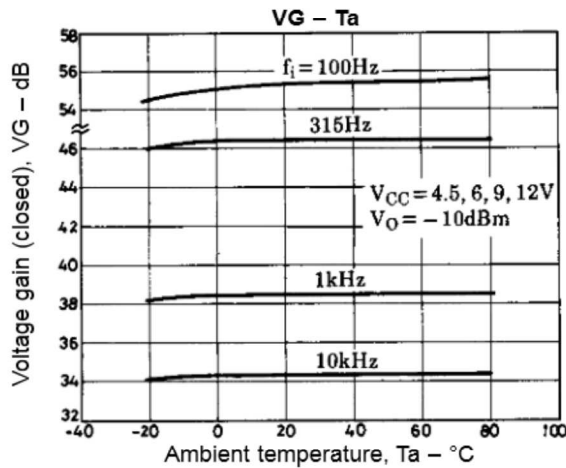
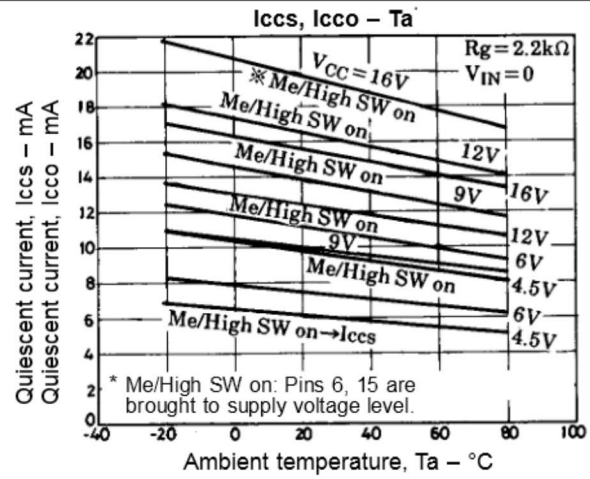
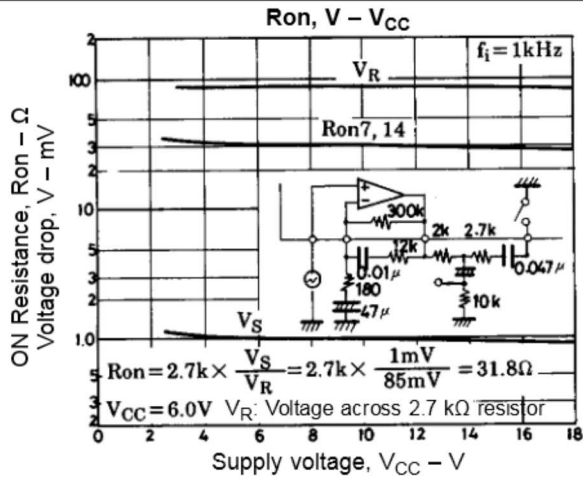
CH1 Crosstalk (between forward and reverse), CT7 – dB



CH2 crosstalk (between forward and reverse), CT8 – dB

Output noise voltage, $V_{NO} - \mu\text{V}$ 





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